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Towards design space exploration of industrial distributed cyber-physical systems

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Citation

Saadatmand, F. S. (2026, September 30). *Towards design space exploration of industrial distributed cyber-physical systems*. Retrieved from <https://hdl.handle.net/1887/4310251>

Version: Publisher's Version

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Downloaded from: <https://hdl.handle.net/1887/4310251>

Note: To cite this publication please use the final published version (if applicable).

Chapter 7

Summary, Discussion, and Future Directions

7.1 Summary of Challenges and Contributions

This thesis addresses the growing need for a scalable and automated DSE methodology tailored to complex industrial dCPS such as the ASML TWINSKAN machine used as a case study in the thesis. To this end, the proposed CompDSE methodology systematically tackles five core scientific challenges.

First, to overcome the lack of a coherent and scalable framework for efficient DSE focused on performance evaluation in complex industrial dCPS (challenge **CHL1**), we introduce a structured methodology that combines system-level modeling, automated model derivation and transformation, and discrete-event simulation for evaluation.

Second, to support abstract yet accurate system modeling (challenge **CHL2**), we define models for the application workload, the computing hardware platform, and the workload-to-platform mapping. These models are sufficiently abstract to enable efficient exploration while remaining accurate enough to yield meaningful insights.

Third, we identify the necessary execution traces and develop algorithms to automatically derive the aforementioned models from traces collected during real system operation (challenge **CHL3**), thereby eliminating the need for software source code analysis, which is often impractical in industrial contexts.

Fourth, we implement model-to-model transformations and code generators (challenge **CHL4**) to produce simulation-ready entities, thereby enabling rapid performance analysis in a target simulation environment. In this thesis, the OMNeT++ environment has been targeted because it supports a hierarchical module structure, event scheduling, and message passing between components, making it suitable for simulation of large-scale distributed systems with complex interactions.

Finally, to capture intra-process parallelism alongside inter-process parallelism

(challenge **CHL5**), we propose a refined application workload model by grouping cohesive computation and communication events into semantically meaningful execution blocks as well as a dependency analysis approach to detect which blocks within a process can execute safely in parallel.

Through experiments on real trace data collected from the ASML TWINSKAN machine, we demonstrate the accuracy and efficiency of the proposed CompDSE methodology. It enables efficient performance evaluation of large-scale workloads and supports insightful system architecture exploration for realistic industrial settings.

7.2 Discussion and Future Directions

While the CompDSE methodology offers a practical and generalizable framework for the DSE of large-scale industrial dCPS, several limitations and open directions have emerged during its development and evaluation. These can be framed as key challenges for future work.

Partial Traceability of Subsystems

Due to system constraints, we may be unable to trace all subsystems to automatically derive models. Some subsystems are bare-metal and lack an OS or another infrastructure with tracing facilities. Thus, such untraceable subsystems have been grouped into the ENV model. In addition, some embedded subsystems, although they are traceable, they cannot store large traces locally, similar to most resource-constrained embedded systems. As a result, trace data has to be streamed over the communication network, which introduces bandwidth bottlenecks. In our ASML TWINSKAN case study, it is not feasible to trace more than seven subsystems without disrupting the system operation. Even tracing these seven subsystems requires careful configuration of local buffer sizes, streaming rates, and other parameters.

One possible direction to solve the aforementioned tracing problem could be to repeat the same system operation multiple times under the same configuration and operation mode, and then aggregate the resulting partial traces to automatically derive a more complete application workload model. However, such an approach poses challenges because according to ASML engineers, the system's operational determinism, i.e., executing the exact same workload order across several runs, cannot always be guaranteed. As a result, aggregating traces across executions may introduce inconsistencies. In practice, however, these variations are typically limited in magnitude

and appear as small execution-level differences, which may fall below the resolution of the abstracted workload model and therefore do not prevent meaningful comparative analysis across design alternatives within the defined design space.

Unmodeled Shared-Memory Communication

While the majority of inter-process communication in the ASML TWINSKAN machine is captured through message passing, a small subset of interactions rely on shared-memory communication. These interactions are not traced and modeled in this work. Although their impact on the system model accuracy is minimal in our case, other dCPS in which shared memory communication plays a more significant role may require explicit modeling of such communication to ensure accurate performance analysis.

Events Signatures in Application Workload Model

In our CompDSE methodology, we estimate the workload signature of the computation and communication events using CPU cycle counts as an approximation of execution cost. This abstraction captures only the computational demand of events on a CPU and omits important factors such as cache behavior, memory access latency, and other architectural interactions that may significantly affect actual execution time of events.

This simplification also limits the DSE to hardware platforms with CPU-based computing architectures. As a result, the CompDSE methodology cannot be directly applied to evaluate systems that include alternative computing architectures and components such as GPUs or FPGAs for example. A promising future direction is to develop a mapping approach based on empirical measurements that enables the translation of execution costs (signatures) of events across heterogeneous platforms. For example, by deriving mathematical functions or learning ML models that approximate how execution signatures of events change between different architecture components, CompDSE could be extended to explore a broader hardware platform design space.

Simplified Scheduling for Processes

In this work, we employ a FCFS scheduling policy to schedule the processes mapped onto a given host, while the real ASML TWINSKAN system employs a more complex, priority-based scheduling. Although this simplification does not significantly impact the accuracy of our performance analysis for this system, the same may not hold for other dCPS that operate under hard real-time constraints for example. In such

systems, accurately modeling the scheduling policy, potentially replicating the real-time scheduler used in deployment, may be essential to ensure reliable performance analysis.

Communication Network Model Simplification

Our communication network model within the hardware platform model relies on approximated communication delays associated with communication events. While this high level of abstraction is sufficient for our case study to explore computing hardware platforms and workload-to-platform mappings, it restricts the fidelity with which alternative network architectures can be evaluated. Although the design space defined in Section 3.6 allows modifications to the network topology, such variations are assessed at the abstraction level of the adopted communication model. Detailed protocol behavior, routing dynamics, and fine-grained contention effects are not explicitly represented. Consequently, the impact of topology changes on communication load and overall system performance can only be analyzed in terms of abstract latency and bandwidth parameters rather than detailed network-level effects.

Scope and Limitations of the Explored Design Space

The design space defined in this thesis is intentionally scoped to what can be evaluated efficiently using abstract models. This scoping reflects a trade-off between accuracy and scalability, i.e., increasing model details may improve fidelity for specific effects, but it also increases design-point evaluation time and can make DSE impractical for large and complex industrial distributed systems.

Some limitations arise directly from the chosen abstraction level and cannot be removed within the current methodology. In particular, design dimensions that require instruction-level or micro-architectural visibility are fundamentally outside the scope of the current methodology. This includes exploration of cache hierarchies and cache policies, pipeline-related effects, fine-grained memory-access behavior, and other instruction-level mechanisms. Supporting such variations would require instruction-level traces or cycle-accurate models, which conflict with the intended scalability constraints in large industrial environments.

There are additional limitations in this thesis that do not stem from the proposed methodology itself, but from the current instantiation of the models. For example, as discussed earlier, a more detailed communication network model would enable the network architecture and topology to be treated as explicit design dimensions, thereby allowing a broader exploration of design points. Similarly, heterogeneous

compute resources (e.g., GPUs or FPGAs) could be considered at an abstract level if an appropriate equivalence or mapping of computational capability can be established as discussed.

Memory-related design dimensions occupy an intermediate position with respect to these limitations. While detailed memory behavior is strongly influenced by micro-architectural mechanisms, memory effects can, in principle, be incorporated at a higher level of abstraction. For example, memory can be modeled as an abstract shared service characterized by parameters such as bandwidth, and latency, and application workloads can be augmented with abstract memory-demand attributes. Such representations do not aim to capture precise memory access timing, but rather to reflect the relative impact of memory pressure on execution behavior across alternative design points. However, introducing these abstractions requires additional assumptions regarding overlap between computation and memory access, as well as contention effects.

Algorithmic or functional changes in the application software are not treated as direct variation/design points within the defined design space. However, such changes can still be evaluated within the overall workflow by collecting new execution traces and re-deriving the workload model automatically for the modified software, after which the resulting model can be assessed under alternative platform and mapping configurations.

Generality vs. Accuracy in Parallelism Analysis

The refined application workload model enables the identification of inter-process parallelism, i.e., identifying dependencies between execution blocks within a process to reveal potential parallel execution of blocks. To identify such dependencies, we adopt a conservative dependency analysis approach in order to maintain generality, deadlock-free model execution, and avoid reliance on system domain knowledge. However, incorporating system-specific knowledge in the dependency analysis could make it less conservative, thereby revealing more accurately the potential parallelism between execution blocks. For example, in the ASML TWINSCAN machine, the measurement and exposure phases belong to two distinct and independent functional categories. Recognizing this separation could help distinguish independent execution blocks within a process more effectively.

Additionally, in the refined model, the ordering of events within each execution block is kept fixed to ensure correctness. With sufficient domain knowledge, however, this constraint could also be relaxed, allowing events within a block to be reordered or

executed in parallel, thereby revealing further opportunities for parallelism.

Evolving the Δ Parameter Model into Design Variables

The Δ -parameter approach is introduced to capture the timing impact of untraced embedded hosts that interact with the physical environment via sensors and actuators. Two questions arise: Can individual Δ parameters serve as independent design variables in DSE rather than scaling all Δ parameters, as done in the experiments presented in Chapter 6? If so, can the model be reformulated such that the Δ parameter values capture only delays due to the physical environment (sensors and actuators), while excluding execution and communication latency inside untraced subsystems?

In practice, for a complex dCPS, our current approach generates thousands of Δ parameters because each communication with an untraced host is represented individually. The very large number of Δ parameters creates a huge design space that is costly and infeasible to explore. In addition, many of these parameters are dependent, so varying them independently can yield unrealistic or infeasible design points.

A straightforward way to reduce the number of Δ parameters is to increase trace coverage so that fewer interactions remain untraced. However, as explained earlier, tracing additional subsystems has its own challenges, and moreover, some subsystems will remain untraceable anyway. In such cases, a more effective approach can be to incorporate system domain knowledge. The key idea is to identify a small subset of independent Δ parameters as **representative** parameters and to express the remaining parameters as functions of these representatives. Using only the representative parameters as design variables in DSE can reduce the size of the design space significantly and can prevent infeasible or unrealistic design points from being considered. This can decrease the number of Δ parameters and improve the effectiveness and efficiency of DSE when exploring changes in untraced hosts and in sensors and actuators.

Domain knowledge also helps separate Δ parameters that are tied directly to the physical environment from those that arise from execution or communication within untraced subsystems. For parameters that correspond to repeated interactions with the same sensor or actuator within an operation mode, the observed timings are often constant or nearly constant. In such cases a single characteristic value can serve as the representative for that component. If a different sensor or actuator is selected during DSE, only the corresponding representative value needs to change. Consequently, the portion of the Δ parameters that reflects the physical environment becomes a set of well-defined design variables to explore.

Simulation Speed vs. Model Detail Trade-off

By refining the application workload model, we improve the model accuracy but increase the model simulation time by approximately 10 times, with each design point taking around 10 minutes to evaluate. This fact highlights the need to carefully balance between the model accuracy and model simulation efficiency. Future work aiming for higher model accuracy, such as adding more detail to the ENV model, must consider the impact of such model refinement on the efficiency of DSE, especially the time needed for a single design point evaluation.

OMNet++ Scalability Limits

The OMNeT++ discrete-event simulation environment has been chosen in our work due to its strong capabilities in modeling large-scale networks and distributed systems. However, our practical experiments reveal that it has scalability limits in terms of the number of modules that can be simulated. This means that even if we are able to trace all subsystems in a dCPS, it may not be feasible to include all process entities as separate modules in the simulation environment. Therefore, a systematic study is needed to evaluate the suitability of different discrete-event simulation tools for large-scale workloads in complex dCPS, and to identify alternatives or extensions that can scale better.

7.3 Concluding Remark

This thesis concludes a very focused and industry-driven research effort towards enabling DSE for complex industrial dCPS. While this work marks the end of our contribution to this specific line of research, it lays a foundation that can be extended and applied beyond the system studied here.

The proposed CompDSE methodology is not limited to the ASML TWINSKAN machine. Its trace-based modeling approach, algorithms and tools, simulation infrastructure, and refinement techniques are relatively general and can be adapted to other large-scale systems. In this sense, the work takes a first step towards making DSE more practical and accessible in industrial contexts, supporting system architects in evaluating alternative designs early in the development process through efficient system simulation.

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