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Journal of Applied Physics

RESEARCH ARTICLE | MAY 02 2023

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*J. Appl. Phys.* 133, 174503 (2023)
https://doi.org/10.1063/5.0147376

Journal of Applied Physics ARTICLE scitation.org/journal/jap

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Cite as: J. Appl. Phys. 133, 174503 (2023); doi: 10.1063/5.0147376
Submitted: 22 February 2023 · Accepted: 15 April 2023 ·
Published Online: 2 May 2023



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## ABSTRACT

Epitaxial graphene (EG) on cubic silicon carbide (3C-SiC) on silicon holds the promise of tunable nanoelectronic and nanophotonic devices, some uniquely unlocked by the graphene/cubic silicon carbide combination, directly integrated with the current well-established silicon technologies. Yet, the development of graphene field-effect devices based on the 3C-SiC/Si substrate system has been historically hindered by poor graphene quality and coverage, as well as substantial leakage issues of the heteroepitaxial system. We address these issues by growing EG on 3C-SiC on highly resistive silicon substrates using an alloy-mediated approach. In this work, we demonstrate a field-effect transistor based on EG/3C-SiC/Si with gate leakage current 6 orders of magnitude lower than the drain current at room temperature, which is a vast improvement on the current literature, opening the possibility for dynamically tunable nanoelectronic and nanophotonic devices on silicon at the wafer level.



## I. INTRODUCTION

Epitaxial graphene (EG) synthesized on cubic silicon carbide on silicon (3C-SiC/Si) pseudosubstrates could offer the possibility of direct integration with the well-established CMOS technologies for integrated nanoelectronic and nanophotonic applications—some of which are uniquely offered by the combination of graphene and 3C-SiC[1]—with the long sought-after dynamic reconfiguration capability, thanks to graphene's tunable electronic and optical properties.[2–7] One of the most common approaches to tuning graphene's properties is controlling the charge concentration in a top- or bottom-gated configuration.[8,9] When exploring the EG characteristics in gated field-effect transistors (FETs), the leakage current is an important performance indicator that defines the device efficiency.[10,11]

While epitaxial graphene FETs (EGFETs) on hexagonal SiC wafers have been shown to have leakage as low as 50 pA,[12] unfortunately, EGFETs on 3C-SiC/Si substrates have typically suffered from substantial leakage to the extent that the gate voltage control becomes inefficient.[13] In fact, in the 3C-SiC/Si pseudosubstrates case, we have additional key challenges: (1) the coverage and uniformity of the EG as well as (2) the quality and control of the 3C-SiC/Si substrate heterointerface.[2,4,9–11,14]

A few attempts were made to fabricate EGFETs on 3C-SiC/Si using EG formed by thermal decomposition of 3C-SiC via resistive heating of the conductive 3C-SiC/Si substrate (at ∼1200 °C in ultra-high vacuum)[13,15–20] as shown in Fig. 1(a). Kang *et al.*[13] fabricated top-gated EGFETs on 3C-SiC(111)/p-Si(111) and indicated current conduction through the 3C-SiC layer and the Si substrate and a significant amount of gate leakage current. The same group reported on back-gated FETs based on 3C-SiC(110)/p-Si(110),[21] which were again limited by a significant amount of leakage current due to the defective SiC layer. Moon *et al.*[22] reported on top-gate FETs using EG on Si(111) wafers but using 35 nm $SiO_2$ as a gate oxide. However, none of these works addressed and solved the issues of the inconsistent EG coverage on 3C-SiC/Si via thermal decomposition and that of the unstable, leaky 3C-SiC/Si heterointerface.

In this work, we approach the EG growth using a catalytic alloy of Ni (10 nm)/Cu (20 nm) onto 3C-SiC/high-resistivity silicon pseudo-substrates; see Fig. 1(b).[2,14,23,24] The alloy-mediated approach enables a consistent EG coverage over large areas despite the highly defective heteroepitaxial 3C-SiC surface thanks to liquid-phase epitaxial growth conditions, as opposed to the more conventional EG synthesis by thermal decomposition of the 3C-SiC.[23]

In addition, a recurring issue in the EG formed on a 3C-SiC/Si heterojunction system is the instability of the rectifying p–n junction between the p-type Si and the unintentionally n-typed doped 3C-SiC.[2,14,25] The carrier inversion phenomenon of 3C-SiC to p-type due to the formation of an electrically active interstitial carbon behaving as acceptor traps within the silicon matrix has typically led to substantial electrical leakage.[14,25] In this work, we prevent the typical 3C-SiC/Si interface leakage by using highly resistive 3C-SiC on a highly resistive silicon substrate, which ensures thorough electrical insulation of the EG from the substrate.[2,4]

We, hence, demonstrate top-gated EGFETs on cubic silicon carbide on silicon with a gate leakage current at least 6 orders smaller than the drain current at room temperature, a necessary requirement for envisaging tunable devices, which was previously unattainable.

## II. GRAPHENE SYNTHESIS AND FET FABRICATION

We use unintentionally doped, 500 nm NOVASiC 3C-SiC films epitaxially grown on 235 $\mu$m thick highly resistive (resistivity > 10 kΩ cm) Si (100) substrates. Prior to the graphene growth, the 3C-SiC/Si substrate wafers are diced into $1.1 \times 1.1$ cm$^2$ coupons and cleaned in acetone and isopropanol. The alloy-mediated epitaxial graphene growth was performed via a solid source method using nickel and copper as catalysts and annealing at 1100 °C, $5 \times 10^{-4}$ mbar, as reported elsewhere.[23,24] After annealing, the samples undergo a wet Freckle etch (∼16 h) to remove the metal residues and silicides. This results in few-layer graphene, i.e., 3–7, as indicated elsewhere.[2]

Figure 2 shows the fabrication process flow for the EGFET. The source(S)/drain(D) electrodes [Au (100 nm)/Ti (10 nm)] are obtained via a lift-off process using a 300 nm thick stack of a bi-layer PMMA resist patterned with 100 kV electron beam lithography (EBL, Raith EBPG5150). Next, the dielectric stack is formed via RF sputtering covering the entire wafer surface. This study compares two types of gate dielectric stacks: one using only 50 nm $SiO_2$ and the other using 10 nm $Si_3N_4$ between the EG and the 50 nm $SiO_2$. This is to evaluate and screen out potential effects of the direct contact of the $SiO_2$ gate dielectric, including an additional charge transfer[26] with a thin nitride layer. Next, the drain-source channels and vias are patterned with EBL using 300 nm thick ARP6200.9, followed by RIE etching. The device was slightly over-etched on purpose. Finally, also the gate electrode consisting of Au (100 nm)/Ti (10 nm) was similarly obtained via e-beam evaporation and lift-off.

The electrical characteristics of the EGFETs were measured at room temperature with a Keithley 4200A-SCS semiconductor parameter analyzer and a C-2 mini probe station from Everbeing International Corporation. Samples were also electrically characterized in a Lakeshore TTPX probe station at room temperature under $1.7 \times 10^{-4}$ mbar vacuum, and gate leakage measurements were performed using a Keithley 2400 source meter.



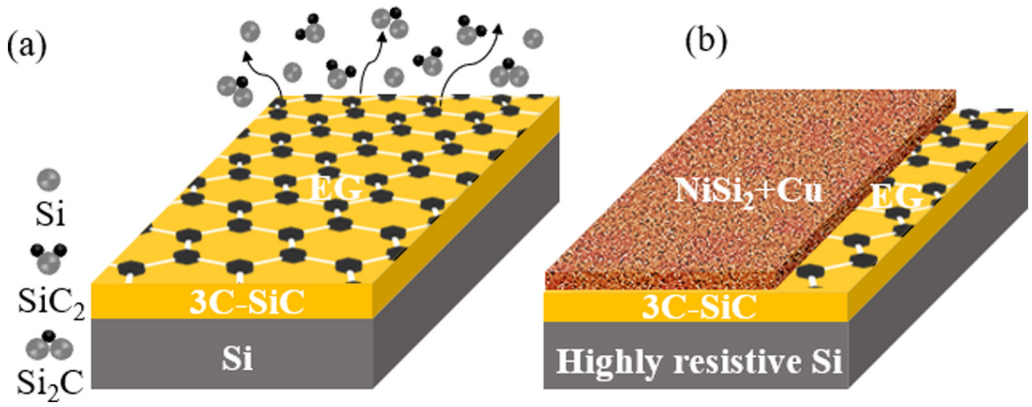


**FIG. 1.** Synthesis of epitaxial graphene on 3C-SiC on silicon substrates via (a) thermal decomposition of 3C-SiC via resistive heating of the conductive 3C-SiC/Si substrate[20] and (b) a catalytic alloy-mediated approach using 3C-SiC/highly resistive silicon used in this work.[23]

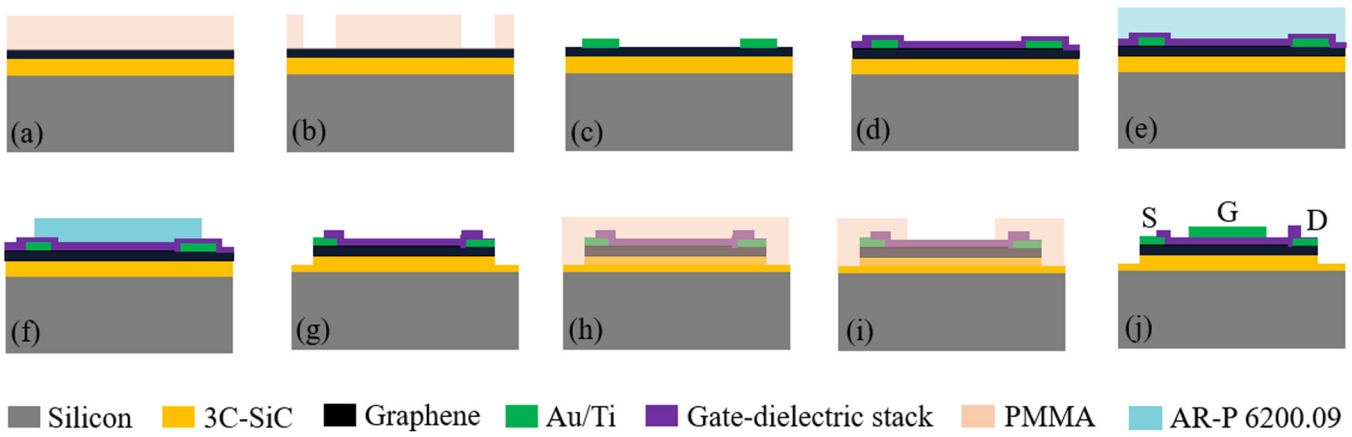


**FIG. 2.** Fabrication process flow for the top-gated EGFETs on 3C-SiC/Si (a) and (b) spin coating 400 nm of bi-layer PMMA and EBL patterning, (c) e-beam evaporation of Au (100 nm)/Ti (10 nm) and lift-off, (d) RF sputter coating of gate dielectric stacks $SiO_2$ (50 nm) or $SiO_2/Si_3N_4$ (50 nm/10 nm), (e)–(g) spin coating of 300 nm of AR-P 6200.09 and EBL patterning, followed by dielectric and graphene etching by RIE (h)–(i) spin coating of 400 nm of bi-layer PMMA and EBL patterning and development of PMMA for gate electrode deposition. (j) e-beam evaporation of Au (100 nm)/Ti (10 nm) and lift-off.

## III. RESULTS AND DISCUSSION

Figure 3(a) shows the optical microscopy image of the graphene channel with length, $L = 10\,\mu m$, and width, $W = 5\,\mu m$, between the S/D contacts of an EGFET, and Fig. 3(b) shows the average Raman spectra of the graphene channel (across a $1 \times 3\,\mu m^2$ area) indicating the D, G, and 2D Raman bands of graphene.

As a first step, we compare the effect of having a $SiO_2$ gate dielectric directly on the EG vs the use of a thin $Si_3N_4$ liner between the EG and the $SiO_2$—see Figs. 4(a) and 4(b). Figure 4(c) shows the gate leakage current for the EGFETs at $V_{DS} = 0$ V for both gate dielectric approaches. The data indicate a significant amount of electrical leakage current in the order of $10^{-6}$ A when the gate dielectric is only $SiO_2$. This high leakage is likely due to the presence of electrically active defects within the $SiO_2$, which may have been introduced during the $SiO_2$ deposition process via the RF sputtering.[27] In contrast, when the $Si_3N_4$ gate dielectric layer is between the $SiO_2$ and EG, the gate leakage is 6 orders of magnitude smaller and in the order of $10^{-12}$ A. This is attributed to lower defectivity and a higher dielectric constant of $Si_3N_4$ (7), which acts as a protective barrier and electrically insulates the EG.[28–30]

To further confirm the leakage current measurements for the gate dielectric stack comprising both $SiO_2$ and $Si_3N_4$ in Fig. 4, we performed gate leakage measurements at room temperature in $1.7 \times 10^{-4}$ mbar vacuum on the EGFET—see Fig. 5. Figure 5 confirms gate leakage current in the $10^{-12}$–$10^{-10}$ A range.



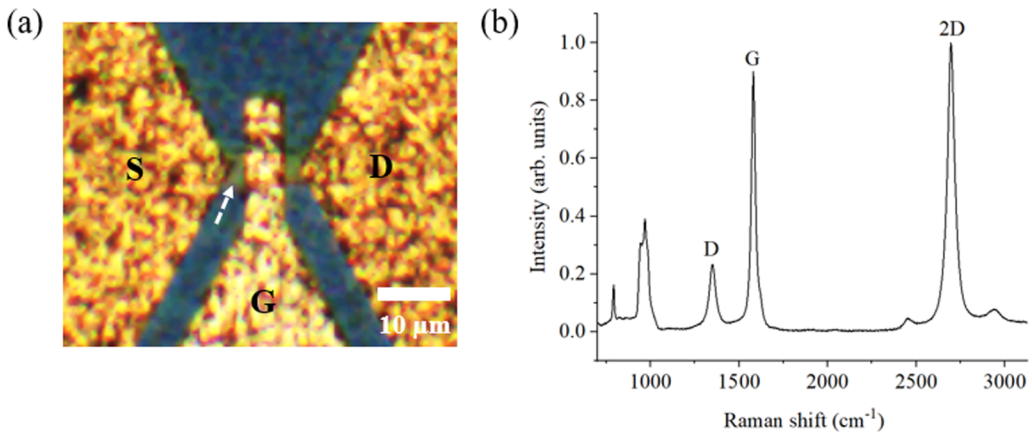


**FIG. 3.** (a) Optical microscopy image of a 10 $\mu$m long and 5 $\mu$m wide graphene channel on EGFET on 3C-SiC/Si. The arrow points to the graphene channel. (b) Raman averaged spectrum across a $1 \times 1\,\mu m^2$ area on the graphene channel after the EGFET fabrication.

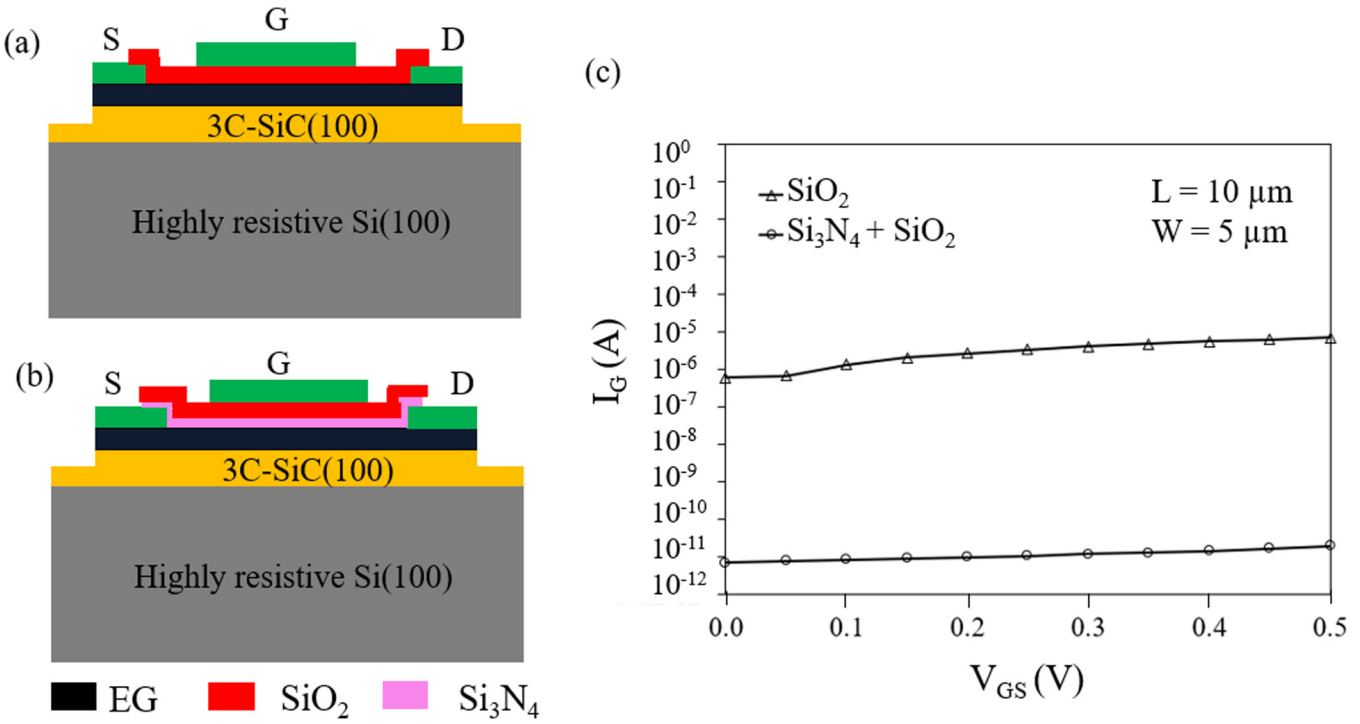


**FIG. 4.** Schematic cross-sectional view of the top-gate FET fabricated with epitaxial graphene on 3C-SiC/Si using (a) only 50 nm $SiO_2$ as the gate dielectric. (b) 50 nm $SiO_2$ with 10 nm $Si_3N_4$ in between the EG and $SiO_2$. (c) Compares $I_G$ vs $V_{GS}$ at $V_{DS} = 0$ V for the EGFETs fabricated with the two gate approaches.

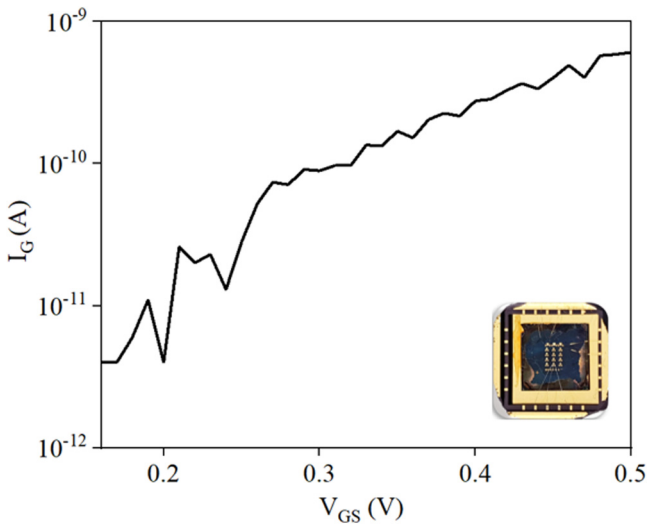


**FIG. 5.** Gate leakage measurements at 300 K, $1.7 \times 10^{-4}$ mbar vacuum on EGFET at $V_{DS} = 1.6$ mV. (The inset shows an optical microscopy image of a wire bonded EGFET.)

In the paragraphs below, we focus on the EGFETs with the gate dielectric stack of both $Si_3N_4$ and $SiO_2$. Figure 6 shows the transfer characteristics of the EGFET at room temperature.

The drain current $I_D$ decreases monotonically as the gate voltage $V_{GS}$ increases, indicating p-type conduction in the EG.[31] This is consistent with the conduction type obtained from room temperature transport characteristics of EG/3C-SiC/Si(100) grown with the Ni/Cu alloy approach.[2] Previous work had shown holes as charge carriers with a sheet carrier concentration in the range of $\sim 10^{13}$ cm$^{-2}$ at a Fermi level of ~0.55 eV away from the Dirac point.[2] Wei *et al.*[31] have reported that the Dirac point for highly p-type doped graphene occurs at higher positive values of $V_{GS}$. To remain safely away from the thin dielectric breakdown region, here, we cannot demonstrate the ambipolar conduction.

Figure 6 also demonstrates that the gate current, $I_G$, in the EGFET device is ~6 orders smaller than the drain current. We believe that this is a vast improvement compared to the literature as Kang *et al.*[13] have reported gate current only 2–3 orders smaller than the drain current for EGFETs on 3C-SiC/Si(111) with 10 $\mu$m long and a 20 $\mu$m wide channel and a 200 nm SiN layer as a dielectric.

The field-effect mobility, $\mu$, of the EGFET is given by $\mu = L/W \times 1/C_G \times 1/V_{DS} \times (dI_D)/(dV_{GS})$.[12,32] The value of $(dI_D)/(dV_{GS})$ is 0.3 $\mu$AV$^{-1}$.[8,9] $C_G$ is the gate dielectric capacitance per unit area, which is given by $(\varepsilon_o \times \varepsilon_d)/t_{ox}$, where $\varepsilon_o$, $\varepsilon_d$, and $t_{ox}$ are permittivity

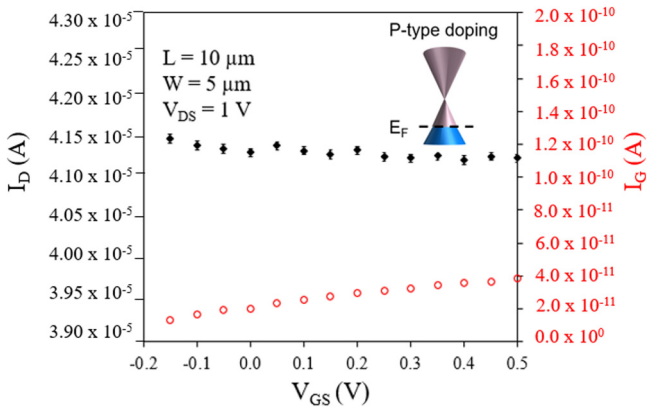


**FIG. 6.** Transfer characteristics of the EGFET at $V_{DS}$ = 1 V.

of the free space, permittivity of the gate dielectric layer, and thickness of the gate dielectric layer, respectively.[12,22] According to 50 nm top $SiO_2$ ($\varepsilon_d = SiO_2 = 3.9$) on a 10 nm $Si_3N_4$ ($\varepsilon_d = Si_3N_4 = 7.5$) gate dielectric structure, the $C_G$ is $4.43 \times 10^{-8}$ F cm$^{-2}$. Hence, the mobility can be calculated as ~14 cm$^2$ V$^{-1}$ s$^{-1}$. Note that this value of field-effect mobility is in the same order as the van der Pauw–Hall effect mobility for EG/3C-SiC/Si(100).[2] The mobility of the integrated graphene is dependent on the interaction of graphene with its bottom and top interfaces dominating the scattering mechanism. Regarding the bottom interface, suitable intercalation could mitigate the strong coupling of the epitaxial graphene with the underlying silicon carbide to improve mobilities.[33–35] Regarding the top interface, Liao and Duan[36] reported that the interfacial phonon scattering can be at least partially screened, resulting in improved mobility, using high-dielectric-constant materials as gate insulators. Gebert *et al.*[37] found that passivating graphene with $Ga_2O_3$ (dielectric constant ~ 10) can efficiently suppress interfacial phonon scattering and greatly improve the mobility of charge carriers in graphene. The sheet resistance of graphene can be estimated from the channel resistance, $R_{channel}$, as $R_s = R_{channel} \times (W/L)$.[38] The $R_{channel}$ can be obtained from $(dV_{DS})/(dI_D)$ in the linear region,[39] resulting in a value of $R_s$ = 16.6 kΩ/sq. Note that in this work, we have not optimized the contact resistance of graphene, which we expect to be elevated.[40] Nevertheless, the graphene sheet resistance estimated from the EGFET characteristics is only about 2.6× times the theoretical maximum sheet resistance, which is roughly $h/4e^2 = 6.45$ kΩ in highly disordered graphene;[41] hence, the graphene is in proximity of its minimum conductivity regime. Cheng *et al.*[9] reported that the high levels of doping in graphene will broaden the $I_D$ curve around the minimum conductivity point in $V_{GS}$, as is also evident from our Fig. 6. We also estimate the sheet carrier concentration from the EGFET characteristics as $n = 1/(\mu \times R_s \times e)$ as $2.7 \times 10^{13}$ cm$^{-2}$.[8,9,38] This quantity is likely somewhat overestimated if the sample is near the puddle regime[42] but is in reasonable agreement with previous estimates of $2 \times 10^{13}$ cm$^{-2}$ from van der Pauw structures.[2]

## IV. CONCLUSIONS

Epitaxial graphene on a 3C-SiC/Si substrate is of high technological relevance due to its ability to seamlessly integrate with silicon technologies for tunable nanoelectronic and nanophotonic devices. Tunable applications typically require electrical gating; hence, the characteristics of gate-controlled field-effect transistors provide a good indication of the efficiency of the tunability. Field-effect transistors based on EG on 3C-SiC/Si have historically been hindered by substantial electrical leakage, typically only of 2–3 orders smaller than the drain current, strongly limiting the efficiency of electrical gating of the graphene. Here, we show that the extent of this leakage can be dramatically reduced by using a Ni/Cu alloy-mediated graphene synthesis onto a silicon carbide on a highly resistive silicon substrate, suppressing the substantial leakage component arising from the 3C-SiC/Si interface. In addition, we show that by selecting a gate dielectric stack of 50 nm of $SiO_2$ and 10 nm of $Si_3N_4$, we obtain gate leakage 6 orders of magnitude lower than the drain current at room temperature, which is a vast improvement on current literature. We believe that this work opens the possibility of achieving dynamically tunable graphene devices on silicon from antennas to optical and nanophotonic filters, some of which are uniquely enabled by the graphene–silicon carbide combination.

## ACKNOWLEDGMENTS

This work was supported by the ARC Centre of Excellence in Transformative Meta-Optical Systems (No. CE200100010). This work was performed in part at the Queensland node of the Australian National Fabrication Facility, a company established under the National Collaborative Research Infrastructure Strategy to provide nano- and micro-fabrication facilities for Australia's researchers. The authors acknowledge the facilities, and the scientific and technical assistance, of the Australian Microscopy & Microanalysis Research Facility at the Centre for Microscopy and Microanalysis, the University of Queensland. M.G., S.B., and M.S.F. were supported by the ARC Centre of Excellence in Future Low-Energy Electronics Technologies (No. CE170100039). We also gratefully acknowledge scientific discussions with Dr. D. Kurt Gaskill.

## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

**Pradeepkumar A.** Conceptualization (supporting); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (equal); Visualization (lead); Writing – original draft (lead). **H. H. Cheng:** Formal analysis (supporting); Methodology (supporting); Resources (supporting); Writing – review & editing (supporting). **K. Y. Liu:** Formal analysis (supporting); Methodology (supporting); Resources (supporting); Writing – review & editing (supporting). **M. Gebert:** Data curation (supporting); Investigation (supporting); Methodology (supporting); Writing – review & editing

(supporting). **S. Bhattacharyya:** Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Supervision (supporting); Writing – review & editing (supporting). **M. S. Fuhrer:** Conceptualization (supporting); Formal analysis (supporting); Methodology (supporting); Resources (supporting); Supervision (supporting); Writing – review & editing (supporting). **F. Iacopi:** Conceptualization (lead); Formal analysis (supporting); Funding acquisition (lead); Methodology (equal); Resources (lead); Supervision (lead); Writing – review & editing (lead).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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