Towards superconducting spintronics with RuO2 and CrO2 nanowires

Prateek, K.

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Josephson Junctions with CrO_2 Nanowires

Half-metallic systems such as CrO_2 are an ideal candidate to investigate very long range proximity effects in S/F hybrids. Although CrO_2 holds great potential for superconducting spintronics, its metastability at ambient temperatures has slowed research. In this work, we have fabricated CrO_2 junctions with two distinct methods to address this issue. The first method involves removing the Cr_2O_3 layer by standard Ar-etching of the top surface of CrO_2. We evaluated the impact of etching on interface transparency in over many (>50*) devices and observed a very wide spread of interface resistance for the same etch parameters, indicating lack of control and consistency required to observe the desired effects. The second approach employs a protective layer of RuO_2 which was grown in situ with CrO_2 in CVD with customized arrangements. The RuO_2 layer results in low contact resistances of around 1 Ω. However, we found the thickness of RuO_2 to be above 50 nm for a very short growth time of 5 sec. Due to its short coherence length of 12 nm, the considerable thickness of RuO_2 prevents the long range proximity effect in these devices. Further optimization of growth settings is needed to attain the target thickness of around 5 nm.*

6.1. Introduction

The interplay between conventional superconductivity and ferromagnetism in superconductor-ferromagnet (S/F) hybrid structures produces a novel form of equal spin triplet superconducting correlations [1]. The triplets, denoted as $|\uparrow\uparrow\rangle$ and $|\downarrow\downarrow\rangle$ in Dirac notation, have parallel spins. Consequently, they are less affected by the pair breaking due to exchange field in the ferromagnet. This facilitates the propagation of triplet pairs over significantly greater distances within the F layer [2]. The phenomenon known as long range proximity (LRP) effect was first proposed by Bergeret et al. in 2001. Since then, in the last two decades, this field has been studied extensively [3–15], primarily focusing on generation and control of superconducting triplet correlations. The key ingredient in conversion from singlet-to-triplet is the engineering of magnetic inhomogeneity through spin mixing and spin rotation at the S/F interface. Experimentally, magnetic inhomogeneity can be introduced through vertical multilayer stacks with different magnetic materials and magnetization directions (for eg. $S/F_0/F/F_0/S$) [16, 17] or magnetic textures like ferromagnetic domain walls [1, 18–20] or interfaces with magnetic disorder [21, 22]. Triplet supercurrents are by definition spin-polarized, and they bear great promise for a new kind of superconducting electronics, in which not only the charge and the superconducting phase, but also the spin is utilised. Some of the potential applications include : use of the supercurrent to generate a spin torque on a nanomagnet and bring its magnetization into motion which can lead to high-frequency oscillators and cryogenic memories; use of the supercurrent to move domain walls; Josephson φ_0-junction-based phase batteries to provide phase shifts in superconducting circuits [23]; or Josephson diodes where the superconducting critical current of the junction depends on the direction of the current [24].

Half-metallic ferromagnets (HMF) like CrO_2 are particularly interesting due to their ability to sustain remarkably high supercurrents (of the order of 10^{10} A/m^2) over hundreds of nanometers [3, 12, 14]. This is in sharp contrast to conventional ferromagnets like Ni, Co, and Fe, which typically exhibit supercurrents over much shorter distances, in the range of a few tens of nanometers. In 2006, Keizer et. al. first reported spin triplet supercurrent in a Jospehson Junction (JJ) device comprising two s-wave superconducting electrodes of NbTiN separated by distances of up to 1 μm on a 100 nm thick film of CrO_2 grown on a TiO_2 substrate (see Fig. 6.1 (b)). However, they found large spread in the critical currents for different devices which suggested that the mechanism responsible for the singlet to triplet conversion was not very clear. In particular a quantitative analysis, comparing the critical current of HMF-based Josephson junctions with the existing theoretical framework [21], was not feasible. In 2010, Anwar *et al.* reported similar results on CrO_2 films grown on Al_2O_3 substrates with MoGe as superconducting contacts. These devices again had

no built-in triplet generator, and the reproducibility was poor (less than 30%) [12]. Later in 2012, Anwar et al. observed long range suppercurrents on CrO_2 deposited on TiO_2 substrates. A thin sandwich layer of Ni (2 nm)/Cu (5 nm) was used between CrO_2 film and the superconducting MoGe to introduce the necessary magnetic inhomogeneity for spin triplet generation.

The above three work were conducted on 'full-film' devices which suffers from a significant limitation due to presence of grain boundaries and ill-defined current paths and an insufficient understanding of the magnetization state at the local level. Fig. 6.1(c) (top) shows the AFM image of the morphology of a CrO_2 film in which the grain boundaries are clearly visible; while Fig. 6.1(c)(bottom) shows its corresponding MFM image. The contrast in the MFM image is due to stray field and indicates that the magnetic configuration over the film is not homogeneous. This may result in poorly controlled magnetic inhomogeneity at the S/F interface which is crucial for triplet generation. Fig. 6.1(d) shows an $R(T)$ plot for two different junctions based on a CrO_2 wire obtained by Ar etching the full film. One of the junction proximizes while the other junction does not, which suggests poor reproducibility of these junctions.

In 2016, Singh et. al. reported SA-grown CrO_2 nanowires based lateral JJs. A sandwich layer of Cu (or Ag)/Ni at the interface of CrO_2 and MoGe was used to provide the necessary magnetic non-collinearity. The junctions could sustain supercurrents of the order of 10^9 A/m^2 below 5 K for a junction length of 500 nm [25]. The potential of CrO_2 for superconducting spintronics is evident; however, advancements in this area have been hindered due to the metastability of CrO_2 at room temperature. CrO_2 reduces into insulating Cr_2O_3 (see Sec. 6.2 for details) resulting in a poorly controlled S-F interface transparency which is critical for generation of spin triplets. In this study, we have fabricated junction devices with CrO_2 nanowires using two distinct methods to address this issue. The first method employs Ar-etching of the top surface of CrO_2 to remove Cr_2O_3 before depositing the contacts. We have systematically analyzed the effects of etching on the interface transparency between CrO_2 and the contact electrodes comprising Ag/Ni/MoGe trilayer stack by varying the etching time. Similar to the initial studies and contrary to report by Singh *et. al.* we found a lack of reproducibility across multiple measurements for the same growth and etch parameters. In the second method a thin layer of RuO_2 is grown in situ on CrO_2 before contacting the wires. This method demonstrates initial potential wherein very high transparency of interface is achieved. However, the growth of the RuO_2 layer, specifically its thickness, needs further optimization to observe LRP effects in the devices. In the following sections both methods of junction fabrication are discussed and the results on them presented.

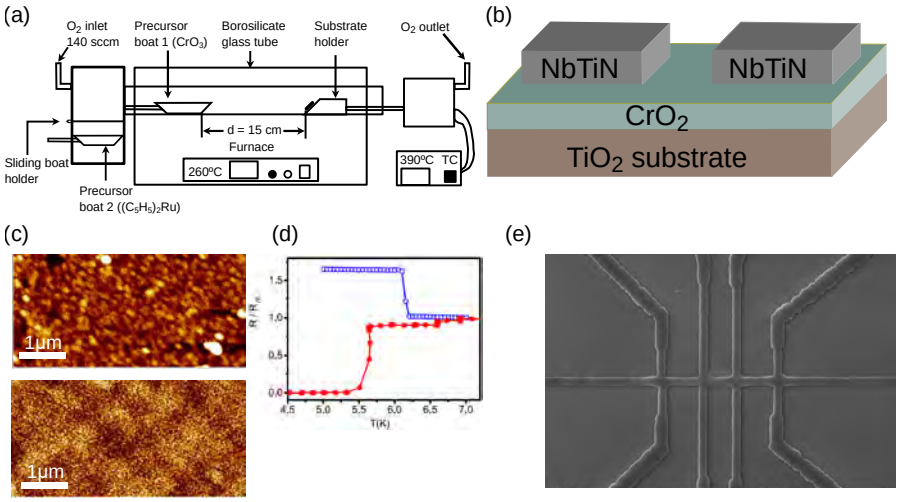

Figure 6.1: (a) Schematic of the CVD setup used for growth of CrO_2. The same setup allows for in-situ deposition of a RuO_2 layer on top of CrO_2. To grow RuO_2, precursor boat1 containing CrO_3 is pulled back out of the glass tube and can be placed in the sealed chamber; and precursor boat2 containing ruthenocene $(C_5H_5)_2Ru$ is introduced in the glass tube. The temperature of the furnace when growing RuO_2 is kept at 80 °C. The substrate temperature is maintained at 390 °C for whole the duration of growth. (b) Schematic of the SFS junction fabricated by depositing superconducting NbTiN electrodes over CrO_2 film on a TiO_2 substrate with lateral gaps of the order of micron. Adapted from Ref. [3]. (c) Atomic force microscopy (AFM) image (top) and magnetic force microscopy (MFM) image (bottom) of a CrO_2 film. The contrast in the MFM image is due to stray fields and shows that magnetic configuration of the CrO_2 film is random, which may result in ill-defined magnetic inhomogeneity at the S-F interface. (d) Resistance vs temperature plot for two junctions based on a CrO_2 wire, obtained by Ar etching the full film, shows the poor reproducibility of these junctions. The success rate of CrO_2-film junctions was less than 10%. Taken from Ref. [25]. (e) SEM image of a selective area grown CrO_2 nanowire. Making junctions based on SA-grown nanowires should result in more control over the local magnetization due to shape anisotropy. *Schematic not drawn to scale.

6.2. Experimental details

As mentioned above, CrO_2 is metastable at ambient conditions and decomposes to a more thermodynamically stable Cr_2O_3 state, which is antiferromagnetic and an insulator [26, 27]. Cheng et al. used photoemission and inverse photoemission to characterize the thickness of Cr_2O_3 layer and they found it to be much thicker than the oxygen core level photoelectron mean free path (around 2 nm) for organometallic chemical vapor deposition grown CrO_2. This insulating barrier prevents developing a good metallic contact on CrO_2 and complicates the fabrication process. From angle resolved x-ray photoemission (ARXPS) and ultraviolet photoemission experiments, it is known that the deposition of transition metal on CrO_2 surface leads to further oxidation and reduction, making the metal-CrO_2

interface very inhomogeneous [28].

Since CrO_2 is metastable, conventional methods for film growth such as sputtering, pulsed laser deposition, or molecular-beam epitaxy cannot be used. Instead chemical-vapor deposition (CVD) has to be employed which prevents in-situ deposition of a protective metal layer over CrO_2. Furthermore, cool-down in the CVD furnace is already an uncontrolled event that may start the Cr_2O_3 conversion. In this work, CrO_2 based lateral S−F−S Josephson junctions (JJs) devices were fabricated using two different approaches to work around the Cr_2O_3 layer problem, which will be discussed in the following sections. Both methods start with the growth of epitaxial CrO_2 wires along [001] direction on a TiO_2 (100) substrate using the Selective Area growth technique via chemical vapor deposition (CVD). Schematic of the CVD set up is shown in Fig. 6.1 (a). and details of the growth process has been described in Chapter 3.2.

For the first method (see Fig. 6.2(a)), CrO_2 wires were grown followed by patterning desired contacts using e-beam lithography. The top surface of CrO_2 was then etched using an argon (Ar) plasma to remove the Cr_2O_3 layer prior to contacts deposition. The tri-layer contacts comprising Ag (5 nm), Ni (2 nm) and the superconductor $Mo_{70}Ge_{30}$ (150 nm; for simplicity called MoGe) were sputter deposited at a pressure of 5×10^{-3} mbar. This was followed by a lift-off process. The etching was carried out in the same sputtering system without breaking the vacuum by reversing the polarity of the plasma, using a pressure of 5×10^{-3} mbar and a bias voltage of 700 V. The Ag (or Cu) acts as a spacer layer and is used to decouple the two ferromagnets. Ni acts as a mixer layer and is used to achieve magnetic inhomogeneity at the interface. By ensuring Ni magnetization perpendicular to the CrO_2 wire, maximum possible magnetic non-collinearity at the S-F interface can be achieved, resulting in an efficient triplet Cooper pair generation.

In the second approach, Ag was substituted with a layer of RuO_2 which is a weak antiferromagnet and a metal. RuO_2 is inert when exposed to typical atmospheric conditions, and can be deposited epitaxially on top of CrO_2 (see Fig. 6.1 (a)) due to their similar lattice parameters. To grow RuO_2 specific arrangements were made in the CVD set up to accommodate the two precursors boats which can be introduced into the glass tube sequentially without affecting the other precursor using the sliding holder. Initially, CrO_2 is grown as shown in Fig. 6.1 using the precursor boat1 in the glass tube. The furnace temperature is set at 260 °C. After the growth of CrO_2 is finished, precursor boat1 containing CrO_3 is pulled back out of the glass tube and can be placed in a closed chamber by shifting the sliding holder up. The temperature of the furnace is brought down to 80 °C. After that, precursor boat2 containing ruthenocene is placed in the glass tube for RuO_2 growth for around 5 sec before boat2 is also removed from the glass tube. The temperature of substrate holder is

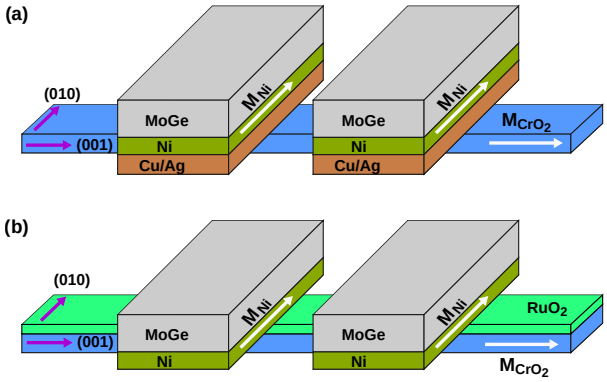

Figure 6.2: Schematic representation of the two different approaches used for fabrication of CrO_2-based lateral S−F−S Josephson junctions (JJs). White arrows indicate the magnetization direction of CrO_2 (M_{CrO_2}) and Ni (M_{Ni}) while purple arrows show the crystal axis. (a) In first approach, the central CrO_2 wire (blue) is first etched to remove the insulating oxide layer of Cr_2O_3 and then tri-layer contacts comprising Cu or Ag/Ni/MoGe were deposited to make the device. (b) In the second approach, a thin layer of RuO_2 was grown in situ on top of CrO_2 wire and then bi-layer Ni/MoGe contacts were deposited without the need of etching. *Schematic not drawn to scale.

maintained at 390 °C for the whole duration of growth. RuO_2 is inert at ambient conditions, so it prevents the formation of Cr_2O_3 and protects the CrO_2 layer, thus eliminating the need for further etching. Next, the contacts were patterned, followed by deposition and lift-off of bi-layer of Ni(2 nm)/MoGe(200 nm).

The fabrication process was followed by the characterization of the device. Initially, two-probe measurements were done at room temperature to check the contact leads, followed by a four-point connection (Current leads: 9-7, Voltage leads: 11-10) as shown in Fig. 6.3(b) (inset)) that allowed a direct measurement of the central CrO_2 wire resistance without the contact wire resistance. Further, electrical and magnetotransport measurements were performed in a Physical Property Measurement System (PPMS) that could be cooled down to a base temperature of 2 K. The magnetic field could be applied along z-axis up to 9 T. We used a Keithley model 6221 low Noise Precision AC/DC Current Source to provide dc current and a Keithley model 2182A digital nanovoltmeter to measure the voltage.

6.3. CrO_2 junctions fabricated by etching process

It is by now well established that a thin insulating layer of Cr_2O_3 forms on top of the CrO_2 surface exposed to atmospheric conditions. To get a comprehensive understanding of the impact of such a barrier on CrO_2 junctions, our initial emphasis

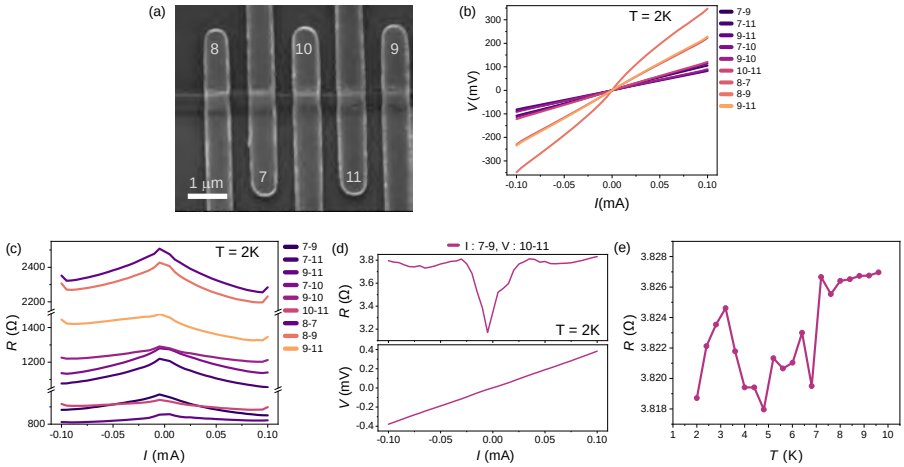

Figure 6.3: No-etch CrO_2 junctions. (a) SEM image of the device consisting of CrO_2 wire of width 370 nm along [001] and multiple contact leads comprising a Ag/Ni/MoGe stack across the CrO_2. The contact leads have edge to edge separation of around 405 nm. (b) Two-point voltage vs current (I-V) plots for different contact configurations on device B measured at 2 K. (c) The corresponding 2 probe resistance as a function of current (R-I). (d) Four-point I-V and the corresponding R-I plot of the central CrO_2 wire. (e) Four-point $R(T)$ measurement between 10 K and 2 K of the central CrO_2 wire between contacts 10-11. A small drop in resistance is observed around T_c of MoGe; after that it oscillates to finally reach 3.818 Ω at 2 K, without a visible proximity effect.

was on a device without etching. This would help with the basic characterization of the device and thereafter serve as a reference point for correlating with the effect of etching of the CrO_2 surface. Subsequently, a series of devices was fabricated with varying etch times in order to determine the optimal time required for our devices. Etching plays a critical role in achieving a good metallic interface between CrO_2 and Ag/Ni/MoGe contact leads. The outcome of underetching is evident as it would result in partial removal of Cr_2O_3 layer. Overetching is also detrimental as it would damage the underlying CrO_2 surface. It should be feasible to manipulate the interface transparency by varying the duration of etching in a systematic manner and identify an appropriate range of etch time for the fabrication of proximized CrO_2 JJs.

6.3.1. Device without etching

In this section, we present the results of measurements conducted on CrO_2 junction device fabricated without etching step. Fig. 6.3(a) shows the scanning electron micrograph of a fabricated junction device consisting of a central CrO_2 wire of width around 370 nm along [001] and multiple contact leads comprising Ag/Ni/MoGe

stack across the CrO_2 wire. The contact leads have lateral edge to edge separation of around 405 nm. To characterize the interface between CrO_2 and contact leads, the device was measured in a 2-probe configuration. Fig. 6.3(b) shows the two-probe voltage vs current (I-V) plots for different contact lead configurations, with the contacts labeled in the SEM image. The measurement (e.g. 7-8 meaning from contact 7 to contact 8) gives the combined resistance of two interfaces. The measurements were at 2 K, which is well below the superconducting transition temperature (T_c) of 6.5 K for MoGe. At 2 K, the measured resistance should have most of the contribution from the interface resistance. While certain I-V curves may appear linear, leading one to assume an ohmic nature of the interfaces, the non-ohmic behavior becomes apparent in the resistance vs current plot (see Fig. 6.3(c)) which indicates that the interfaces are indeed not metallic and the CrO_2 layer is effectively decoupled from the contact leads. Each measurement shows a high resistance of the interfaces, the minimum being above 800 Ω and maximum around 2400 Ω. This suggests local variation among the five interfaces on the same device. We also measured the behavior of the central CrO_2 wire without the contribution coming from contact leads in 4-point geometry. Fig. 6.3(d)) shows the I-V plot (bottom) and the corresponding R-I plot of CrO_2 wire between inner contact leads. The resistance was found to be around 3.8 Ω at 2 K which is typical for CrO_2 wires of such dimensions. However, the R-I plot shows non-ohmic type behavior of the wire, the underlying cause of which remains unclear to us. Finally, we measured 4-point geometry resistance vs temperature measurement on a junction device between 10 K and 2 K as shown in Fig. 6.3(e). The resistance at 10 K is around 3.827 Ω. A small drop in resistance is observed around T_c of MoGe but after that it oscillates to finally reach 3.818 Ω at 2 K and as anticipated, no proximity effect was detected.

6.3.2. Device with etching

After measuring devices without etching, we made a series of devices with different etching times in our quest to find the optimal range. Fig. 6.4(a) shows the resistance vs etch time plot of different devices, measured in a 4-point geometry at 2 K, as the etching time is varied from 0 s up to 90 s. We fabricated multiple devices with the same etch time and in the Figure we chose a random device from the series to represent an etch time. We observed a non-monotonous behavior up to 40 sec of etching beyond which the resistance goes up sharply, suggesting that we are overetching and probably damaging the CrO_2 wire. We found the best results on our devices around 20-25 sec of etch time, but no clear window of the etch times was observed which led to proximization of the CrO_2 junction. This result is contrary to the earlier report by Singh et al. where they found a well defined etching time to see proximity effect [25].

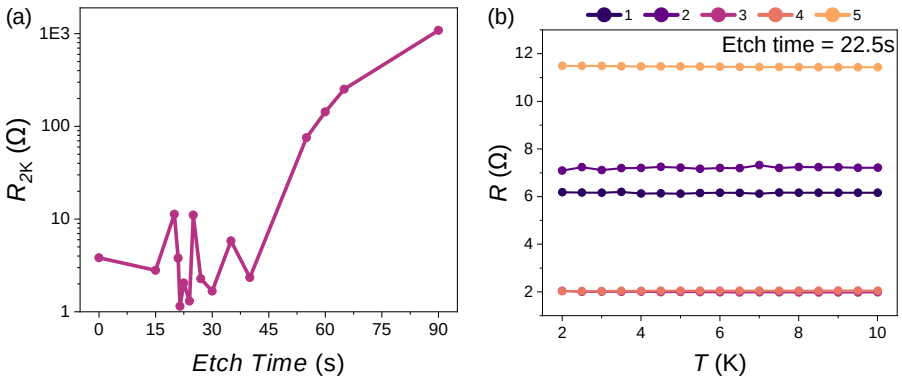

Figure 6.4: (a) Resistance vs etch time plot of different devices measured at 2 K as the etch time is varied from 0 s up to 90 s. Multiple devices were measured for the same etch times, out of which we chose one of the device randomly to be represented in the graph. (b) Four-point resistance vs temperature of CrO_2 wire for five different devices etched for same time of 22.5 s, showing small differences in the measured resistance.

We observed a large spread in interface resistances for the same etching time not only across various devices but even on the same CrO_2 wire. We found interface resistances to be at their lowest for etch time around 20-25 sec. Around this time, the observed interface resistance ranged from as low as 20 Ω to as high as 10 KΩ (not shown in figure). Although the interfaces showed large variations in resistances, we found the 4-point geometry wire resistance (without interfaces) to be consistent. This indicates that the quality of CrO_2 wire is not a factor. Fig. 6.4(b) gives the four-point resistance vs temperature of CrO_2 wire in five different devices etched for same time of 22.5 s. These devices show small spread in the measured resistance which is probably due to small difference in the device dimensions, however none of them showed a proximity effect.

In Fig.6.5, we present the measurements of one of the CrO_2 junction device which was etched for 22.5 s. Fig.6.5 (a) shows the SEM image of the device comprising CrO_2 wire of width (w) = 512 nm, thickness (t) = 65 nm and multiple Ag/Ni/MoGe contact leads. The two inner contact leads are edge to edge separated by 350 nm. Fig.6.5 (b) gives the 2-point I-V (top) and corresponding R-I plots of the contact leads (without interface) measured at 10 K, well above T_c. R-I plots confirm that the contact leads are ohmic and indeed metallic. Subsequently, we measured the device in the quasi 4-point geometry configuration. This configuration allows to measure the resistance of CrO_2 wire along the two interface between CrO_2 and Ag/Ni/MoGe on either side of the central CrO_2 wire (see Fig. 6.2). Fig. 6.5(c,d) show the I-V and corresponding R-I plots in different combinations measured at 2 K. We calculated the interface resistance at each of the four interfaces. Moving from left to right,

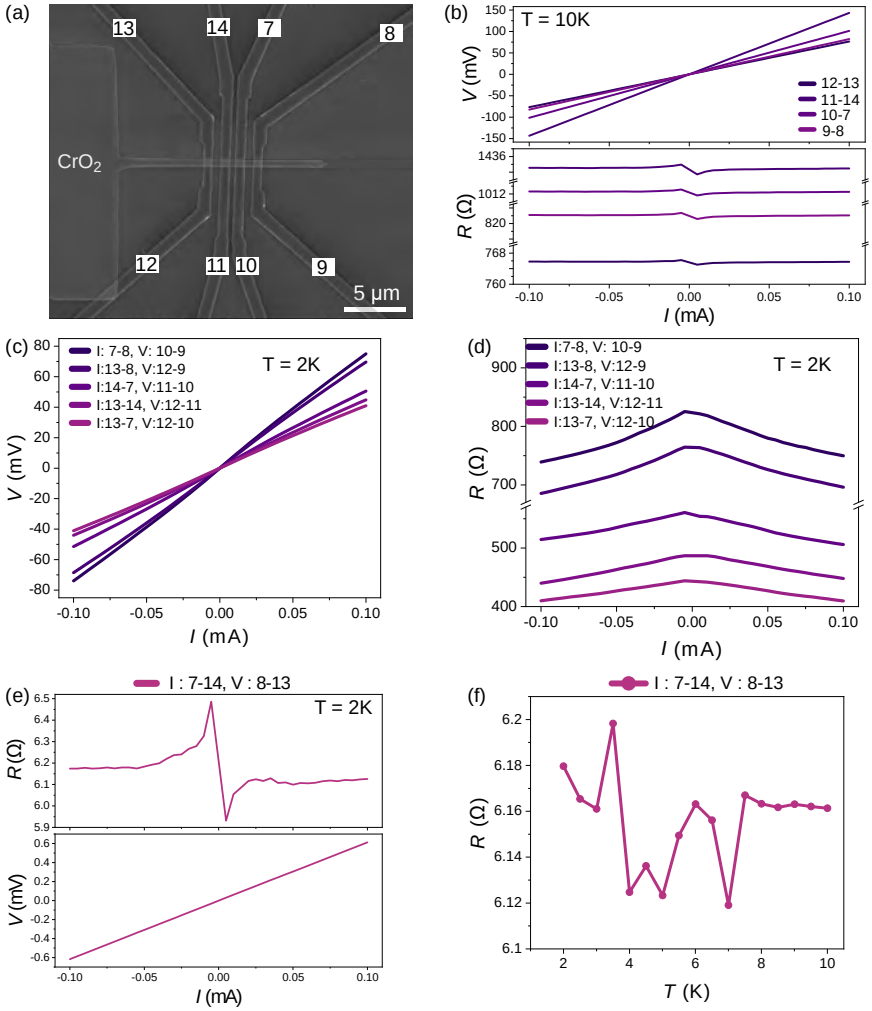

Figure 6.5: SEM image (false color) of one of the CrO_2 junctions fabricated using the first approach of etching the top surface of CrO_2 before depositing tri-layer (Ag/Ni/MoGe) contacts. The two inner contacts are laterally edge-to-edge separated by ~ 350 nm. This device was etched for 22.5 s. (b) 2-point I-V and corresponding R-I plots of the contact leads (without interface) measured at 10 K before T_c. R-I shows good ohmic behavior. (c) Quasi 4-point I-V and the corresponding (d) R-I plot of the central CrO_2 wire and the two interfaces in different configurations measured at 2 K. The interfaces have resistances varying between 400 Ω and 800 Ω. (e) 4-point I-V and the corresponding R-I plot of the central CrO_2 wire without interface. (f) Resistance vs temperature plot of the device between 10 K and 2 K shows the resistance fluctuating around ~ 6.16 Ω.

the resistances were roughly 180 Ω, 300 Ω, 250 Ω and 570 Ω, respectively. We can also calculate the resistance-area product (RA) for these interfaces. From the cross

sectional area of 512×65 nm^2 and interface resistance of 180 Ω, we find an RA of 0.6×10^{-13} Ω.m^2. Similar to the observation on earlier devices, we found a large local variation in resistance among each of the interfaces.

Next, we measured the 4-point I-V and R-I curves (see Fig. 6.5(d)) for the central CrO_2 wire at 2 K. We found that the wire showed typical ohmic characteristics. Finally, we took the resistance vs temperature measurement of the CrO_2 wire between 10 K and 2 K. As expected, a proximity effect was not observed. Instead we found that the resistance fluctuated around 6 Ω after the superconducting transition at 6.5 K. Similar to the above junction device, we measured many (> 50) devices but the interface transparency issue remained unresolved. The earlier studies on proximity effect reported the interface resistance to be around 20 Ω [25]. However, we were not able to fabricate a device with such a low contact resistance, mostly because of the above-mentioned local variation in resistance.

Based on the above observations, we can certainly conclude that the large heterogeneity in resistance not only between the devices etched from same duration but also in the interface resistances of contact leads and CrO_2 wire separated by few hundreds of nm within a single device, limits the precise control required to fabricate a device with a defined resistance. Additionally, the growth of CrO_2 wires based on chemical vapor deposition limits the control of the final shape of the wire in the sense that the top surface of wire is not very flat. Instead we found surface roughness of about 10 nm along the width of the wire when measuring the topography with atomic force microscopy (see Appendix Fig. 6.7). This roughness in turn hinders with control of the etching process of CrO_2 and reliable metallic connection of contact electrodes with high interface transparency, a critical requirement for these junctions.

6.4. CrO_2 junctions fabricated with RuO_2

The lack of control with etching and difficulty to achieve a low interface resistance on our junctions required us to find another approach of fabrication. This is where RuO_2 emerged as a choice of material. The main advantage is that it is a metal, inert in ambient conditions and it can also be grown epitaxially in situ with CrO_2 via CVD due to similar lattice parameters. Further details of growth of RuO_2 can be found in sec. 5.2 In this section, we present the results of measurements conducted on one of the CrO_2/RuO_2 junction device.

Fig. 6.6 (a) shows the false colored SEM image of CrO_2/RuO_2 wire (green) of width around 500 nm and four Ni/MoGe contact leads. The two inner contact leads are laterally edge to edge separated by ~300 nm. Next, one of the contact lead,

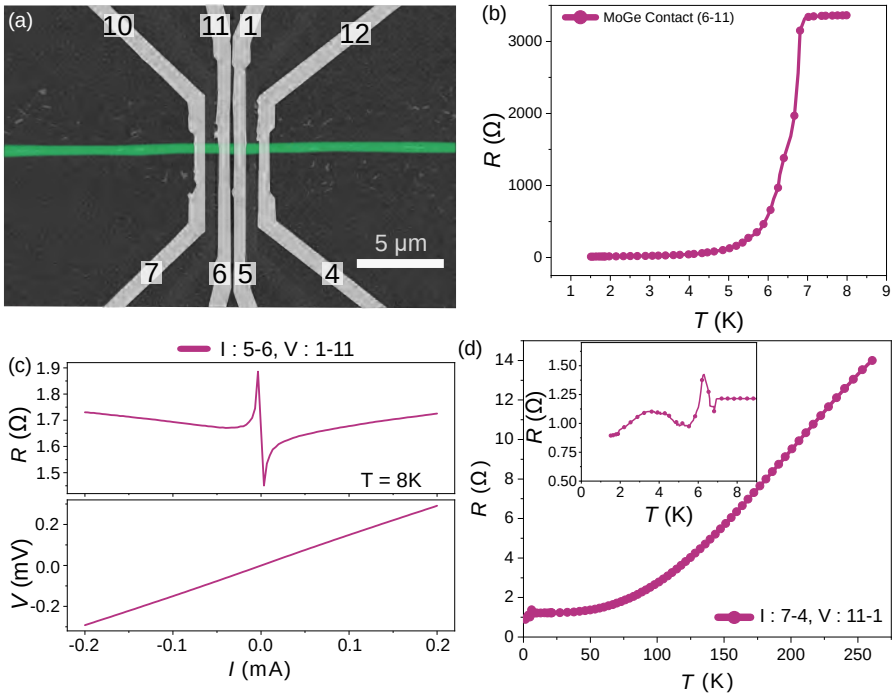

Figure 6.6: (a) SEM image (false color) of a CrO_2/RuO_2 junction fabricated using the second approach where RuO_2 was grown in situ on top of CrO_2 wire, followed by deposition of contact leads comprising Ni/MoGe. The two inner contacts are laterally edge-to-edge separated by ~ 300 nm. (b) 2-point resistance vs temperature plot of contact lead 6-11 shows a superconducting transition (T_c) at T_c of ~ 6.5 K. (c) Quasi 4-point I-V and corresponding R-I plot of the central CrO_2/RuO_2 wire and the two interfaces measured at 8 K before T_c. (d) $R(T)$ plot of the junction measured between 250 K and 1.5 K. The inset shows a small upturn and then a dip in the resistance near T_c of the contact leads. Below T_c the resistance fluctuates around 1 Ω up to 1.5 K.

6-11 was measured in a 2-probe configuration to observe the T_c. Fig. 6.6 (b) shows typical T_c of around 6.5 K. After that, we measured I-V and the corresponding R-I plot (Fig. 6.6(c)) of the central CrO_2/RuO_2 wire and the two interfaces at 8 K. We observed a low resistance value of around ~ 1.7 Ω and a good ohmic behavior from R-I plot, indicating the transparent nature of the interface. Finally we measured $R(T)$ of the junction in 4-point geometry between 270 K and 1.5 K (Fig. 6.6(d)). We observed that the resistance of the device became constant below 10 K (inset), with a values of 1.214 Ω at 7.5 K. When the MoGe contact leads became superconducting at 6.5 K, the resistance started to fall again (after a small dip-peak excursion) but did not reach 0 Ω, indicating that the CrO_2 wire did not proximize completely over the length of the junction. Instead, we observed that the resistance reduced to 0.953 Ω at 2 K, which was nearly 20% decrement from the normal state resistance (R_N) at

7.5 K. This roughly translates to a proximity length of about 30 nm extending from contact leads on either side.

Further investigation into similar junctions fabricated with RuO_2 on top of CrO_2 revealed that the total height of the central CrO_2RuO_2 wire stack is around 150 nm to 180 nm. From our experience with growing CrO_2 for similar duration of time we can safely assume that the thickness of the CrO_2 wire would be ≤ 100 nm. This would mean that the thickness of RuO_2 is ≥ 50 nm. Both CrO_2 and RuO_2 are good metal and have comparable low residual resistance below 10 K. Since the thickness of RuO_2 is quite close to the thickness of the CrO_2 wire, the current would flow through both the materials. However, we know that RuO_2 is a weak antiferromagnet with a short coherence length of around 12 nm (see sec. 5.4). This would hamper the observation of long range proximity effect in these junctions. Ideally, we want to deposit a thin layer (~ 5 nm) of RuO_2 on top of CrO_2 so that maximum current flows through CrO_2. We found that the rate of growth of RuO_2 when growing above CrO_2 layer was very high. Even a growth for ~5 s leads to a thick layer of RuO_2 around (50-80) nm. We tried to change the growth parameters by changing the temperature, oxygen pressure but we did not get the desired outcome. Further investigation into the growth conditions is required to obtain thin RuO_2 wires.

6.5. Summary and Outlook

In summary, CrO_2 based lateral Josephson junctions were fabricated using two different approaches. The first method involved the etching of the top surface of CrO_2 to remove insulating layer of Cr_2O_3. Following this, a stack of Ag/Ni/MoGe contacts was deposited. This method of fabrication demanded a significant level of precision and control throughout various stages, posing challenges in achieving the desired outcomes. Significant resistance variations observed across multiple measurements, without any parameter modifications, indicate a lack of reproducibility. This lack of consistency poses challenges in conducting systematic investigations on the junctions.

The second approach of fabrication using RuO_2 as a spacer layer demonstrate initial potential. The measured devices exhibited high degree of transparency in the interfaces, with interface resistance being as low as 1 Ω. However, the thickness of RuO_2 layer remained a significant concern as it plays a crucial role in the observation of the long-range proximity effect in these devices. Additional research is required to achieve successful control of the growth of thin layer of RuO_2 on top of CrO_2 surface.

6.6. Appendix

6.6.1. AFM image of CrO_2 wire after CVD growth

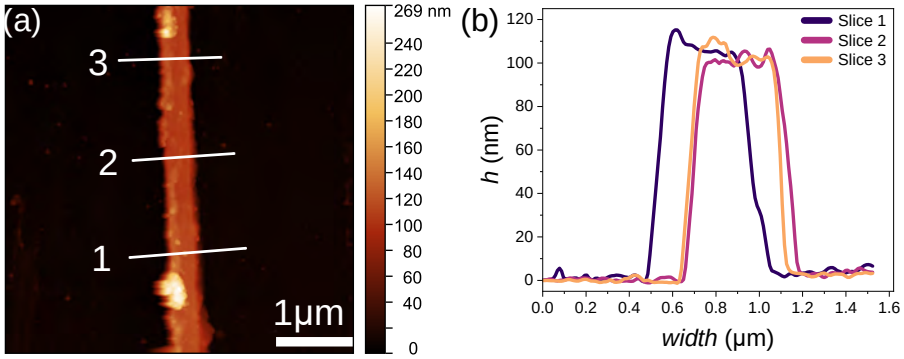

Figure 6.7: (a) Atomic force microscope image of the topography of a CrO_2 wire after CVD growth over an area of 5 X 5 μm^2. 3 slices were taken at random over a cross-section of the wire. (b)Corresponding height profiles of the 3 slices show the uneven top surface of the wire. The maximum roughness is around ~ 14 nm.

The growth of CrO_2 wires using chemical vapor deposition (CVD) has limitations in controlling the ultimate wire shape, in contrast to alternative deposition processes like as sputtering and evaporation. These procedures allow for layer-by-layer deposition, often resulting in the formation of very smooth and flat films. Fig. 6.7(a) gives the atomic force microscope image of the topography of a CrO_2 wire of width (w) $\approx$ 500 nm. We took slices at three different positions on the wire (labeled 1, 2 and 3) and found that the top surface of the wire reveals a lack of flatness. Upon examination, a surface roughness of about 10 nm was detected over the width of the wire, as seen in the line profile of the three slices (Figure 6.7(b)). The presence of surface roughness poses a challenge to the precise control of the etching process of CrO_2 and the establishment of reliable metallic connections between contact electrodes, while maintaining a high level of interface transparency. This need is a critical requirement for the successful fabrication of these junctions.

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