Electrical and magnetic properties of ferritin: electron transport phenomena and electron paramagnetic resonance

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IMPLEMENTATION OF A LOCAL GATE IN WIDE SELF-ALIGNED NANOGAP DEVICES

In this chapter, we report on the fabrication of single-electron transistors by trapping nanoparticles in between self-aligned nanogaps and tuning their conductance through a local back gate. Electrical measurements after gold nanoparticle deposition, below 20 K, show Coulomb blockade-like current vs. voltage characteristics and Coulomb diamonds in the stability diagrams, confirming the presence of a single-electron transistor. The fabrication method can be used to generate single-electron transistors based on different nanoparticles, such as metal/oxide-based particles, and bioparticles.

2.1. INTRODUCTION

The increasing number of applications of small electronic devices in our daily lives (internet of things, mobile phones, biomedical context, industry, etc.) requires substantial power consumption. In this regard, ultra-low power consumption is a hot research topic, where the single-electron transistor (SET) has been considered as a potential candidate to achieve both high-device integration while keeping low power consumption [1].

The idea of the SET was first proposed in 1986, by Likharev and Averin [2]. Until today, different procedures for fabricating a SET have been reported, based on the configuration electrode-island-electrode, involving standard electron-beam lithography and techniques as break junctions [3] and electromigration [4]. In most cases, the electrodes are made of metal (e.g. Au, Pt, Ag) [3, 5]. However, other materials have been explored as well, such as for instance graphene [6, 7]. In any case, an island is needed to connect both electrodes, which can be a nanoobject made of metal [3], graphene [8, 9], a molecule (e.g. porphyrin [6, 7], antibody [10]), molecularly-linked metallic particles [11], or other nanoobjects, as long as the charging energy of the island is larger than the thermal energy, and the tunnel resistances (between the island and the electrodes) are larger than the quantum resistance $R_q = h/2e^2 \sim 12.9\ \mathrm{k\Omega}$.

A fabrication process that can be used for different nanoparticles is desired. A common problem is the placing of the particle in between the electrodes, for which, a combination of dropcasting [12], spin-coating, and dielectrophoresis [3] are commonly used to deposit and trap the particles. However, since the electrode gap area is often small (e.g. in pointy contacts, break junctions), the trapping process is challenging. In this context, wide self-aligned nanogap devices are a feasible candidate to effectively reduce the trapping problem, since the trapping area is at least one order of magnitude greater. Second, these devices allow the trapping of different nanoobjects (metal/oxide nanoparticles, proteins, etc.), making the fabrication process versatile.

The gap in wide self-aligned devices using chromium masks [13] is not defined by direct writing, but is rather the result of chromium oxidation and the corresponding expansion of the mask. Different devices have been reported based on iron-oxide nanoparticles [12], proteins (e.g. ferritin) [14], and spin-crossover nanoparticles, e.g., Prussian blue [15] nanoparticles. Although these devices present a high trapping yield and stable current vs. voltage characteristics at low temperatures, gating in a controllable manner has not been reported. We have used the silicon substrate as a back gate, but the gate coupling is too low to induce a sufficient shift in the electrochemical potential of the 'islands' and thus in the current through them (see Appendix, section 2.5.2).

Here, we report on the fabrication of devices that allow the generation of single-electron transistors. The devices are based on wide self-aligned nanogap devices but include a local gate placed underneath the gap area. To test them, gold nanoparticles of 10 and 40 nm sizes in diameter are used. The current vs. voltage characteristics are stable at low temperatures and confirm Coulomb blockade as the main transport mechanism. Additionally, the gate coupling has a mean of 0.07, allowing the visualization of Coulomb diamond-like features for this size of particles within a gate voltage window of ± 2 V.

2.2. MATERIALS AND METHODS

2.2.1. CHIP DESIGN AND DEVICE FABRICATION

Platinum-wide self-aligned nanogap devices were fabricated on Si/SiO_2 substrates. The spacing between the main electrode (ME) and auxiliary electrode (AE), from now on "the gap", is not defined by direct writing, but it results from a chemical process, in particular, from chromium oxidation. Figure 2.1a shows the chip design: In light blue, the ME (Ti/Pt of 5/30 nm); in dark blue, the 36 AE (Ti/Pt of 5/20 nm); in pink, the local gate electrode (Ti/Pt of 3/13 nm), which is separated from the source-drain electrodes by an insulating hafnium oxide layer (22 nm). The white numbers indicate the labeling order of the devices. Figure 2.1c shows the schematic of a "device", which is the assemblage formed by a pair of ME-AE (depicted as source-drain, respectively), the gap in between them, and the local back gate electrode (GE) below them. The gap length (size) is defined as the shortest distance between ME and AE (red-dotted line, Fig. 2.1c). The gap width is the projection of the AE on the ME (black dotted line), which is 1 μm.

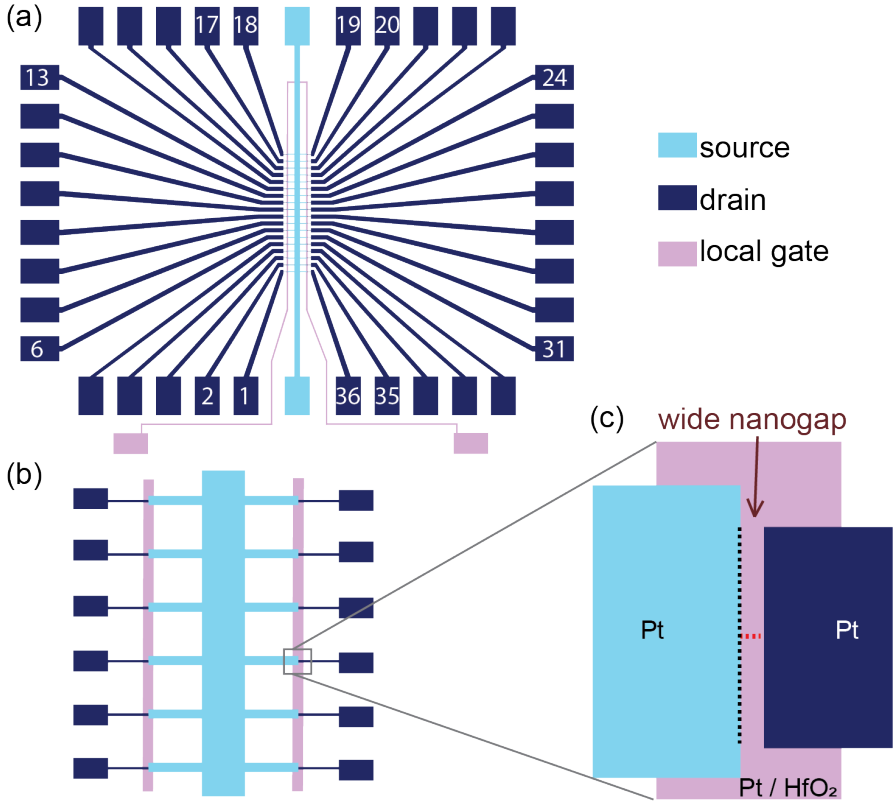

Figure 2.1: Wide self-aligned nanogap chip design. (a) General overview. In light blue, the main electrode (depicted as the source). In dark blue, the auxiliary electrodes (represented as the drain). In pink, is the local gate electrode. (b) Close-up of the center of the chip. (c) Schematic of a "device", formed by the gap, source-drain electrodes, and gate electrode. The gap length/size (8-33 nm) is represented by the red-dotted line. The black-dotted line indicates the gap width (~ 1 μm).

The fabrication of the devices is summarized in Fig. 2.2. On top of a doped Si/SiO_2 substrate, the local back gate electrode (GE) is defined by e-beam lithography (EBL) and evaporation of 3 nm of titanium and subsequently of 13 nm of platinum (Fig. 2.2a-e). The GE is then covered with hafnium oxide deposited by atomic layer deposition (ALD) (Fig. 2.2f). A second EBL cycle defines the ME, by depositing 5/30 nm of titanium/platinum and 20-25 nm of chromium (Fig. 2.2g). Upon oxidation in an oxygen plasma, chromium expands its size. In this manner, chromium oxide acts as a shadow mask of a few nanometers near the edge of the first electrode (Fig. 2.2h). The thickness of the chromium layer and its exposure to oxygen plasma determine the expansion and, thus, the size of the gap. A third EBL cycle defines the AE, by depositing 5 nm of titanium and 20 nm of platinum (Fig. 2.2i). In the final step, the chromium layer is wet-etched away to reveal the underlying nanogaps (Fig. 2.2j).

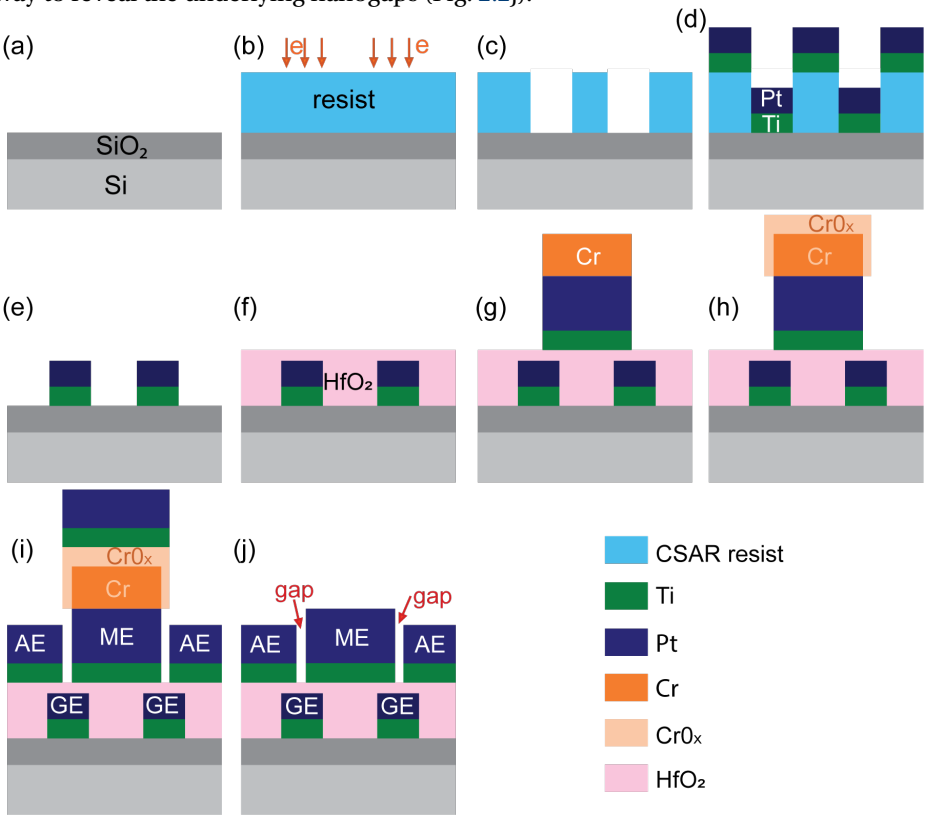

Figure 2.2: Schematic of the fabrication process. (a) Chemical cleaning of a doped Si/SiO_2 wafer. (b) Spin coating and baking of CSAR AR6200 positive resist, followed by e-beam exposure to define the GE. (c) Development in pentyl acetate (1 min.) and wet resist descum (5 s in xylene). (d) Evaporation of Ti/Pt (3 / 13 nm). (e) Lift-off. (f) ALD of hafnium oxide (~22 nm). (g) Second e-beam lithography cycle to define the ME. The evaporation consists of Ti/Pt/Cr (5 / 30 / 25 nm). (h) Chromium oxidation by oxygen plasma, defining the gap size. (i) Third e-beam lithography cycle to define the AE. The evaporation consists of Ti/Pt (5 / 20 nm). (j) Chromium wet-etching (1.5 min.) followed by oxygen plasma for cleaning. The devices are finished.

2.3. RESULTS AND DISCUSSION

2.3.1. DEVICE CHARACTERIZATION

Figure 2.3 depicts two optical images of the top view of a chip before and after chromium etching. The two vertical-light-brown lines are the local GE. Panel (a) displays the chip before the chromium etching process (Fig. 2.2i). In this panel, horizontal thin lines (in beige) can be observed on top of the ME; the latter has been false-colored green to enhance the presence of the thin lines. After etching the chromium (Fig. 2.3b) the central segment of the horizontal lines located on top of the chromium is etched as well, leaving only the two segments at the ends of the lines in place, both separated to the ME by the gaps (red arrow in Fig. 2.4b). Essentially, each horizontal line is aligned with two AEs. Figure 2.4a shows a scanning electron microscopic (SEM) image of the same chip; the red rectangle indicates device #16, whose close-up image is shown in Figure 2.4b.

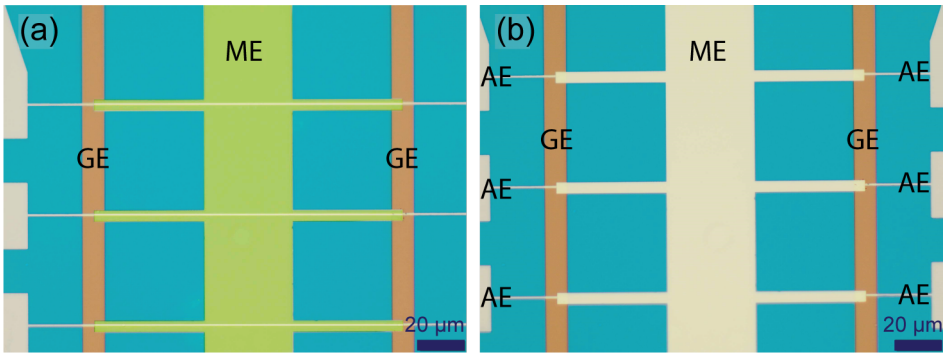

Figure 2.3: Optical microscopic images from chip A (a) before chromium etching (ME false-colored in green), and (b) after chromium etching.

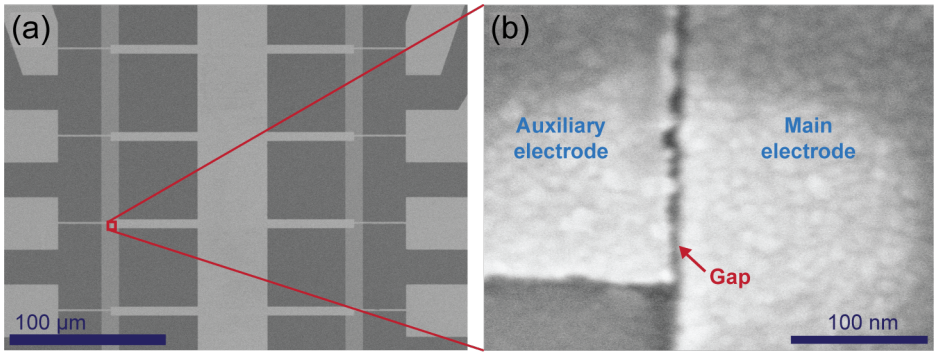

Figure 2.4: Scanning electron microscopic images from chip A shown in Fig. 2.3, after chromium etching. (a) The red rectangle indicates the close-up area of device #16, shown in panel (b). The red arrow depicts the gap between ME and AE. In this particular device, the gap size varies between 8 and 13 nm.

The profile of the source and drain electrodes of a device has been probed by atomic force microscopy (AFM), as illustrated in Fig. 2.5. Panel (a) shows the AFM topographic image. The colored lines (1,2,3) indicate the segments whose height profiles were acquired. These profiles are shown in panel (b), keeping the same color nomenclature as in panel (a). The three profiles were corrected so that their respective lower height level was set to zero. For this, all points that are part of the lower levels were averaged, and that value was set to zero (gray dotted line). Then, to calculate the approximate height of each profile, the mean values of all points placed in the respective upper height level are considered (see colored dotted lines). The blue line measures the ME thickness (height), with an average value of 27.4 nm. The green line indicates the height measurement on the AE (18.0 nm). If we compare the profiles of the ME and AE with the set thickness on the evaporator we see a discrepancy of 7.6 and 7.0 nm, respectively. This mismatch can be attributed to the crystal sensor on the evaporator for various reasons. First, different crystal calibrations result in different readings while using different evaporators or after maintenance. Second, the reading error increases with the use time of the crystal. Therefore, it is not unusual to have differences of 10 nm or less. Finally, the red line is the profile measured by the scan starting on the ME and finishing on the AE, crossing the gap (seen as a spike artifact in Fig. 2.5b); therefore, it is a measurement of the thickness difference between the ME and AE (8.6 nm). Note that the average height of the AE subtracted from the ME is 9.4 nm. This is 8.4% smaller than the average height obtained from the red line. This difference suggests that considering the average value of the data points is a rough rather than an accurate approximation of the measured heights.

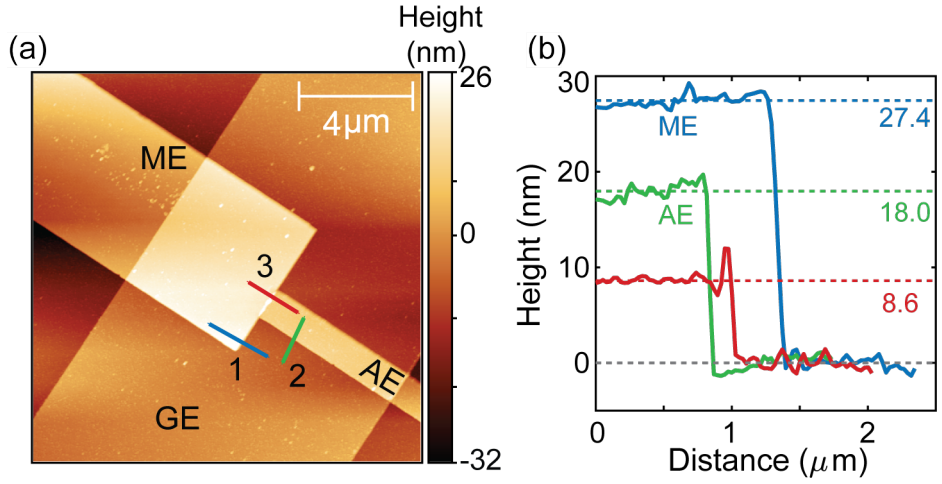

Figure 2.5: (a) Tapping mode AFM image and line profiles obtained from device #7 (chip A) shown in Fig. 2.3, 2.4. (a) Scan directions (colored lines). (b) Height profiles along the colored lines shown in panel (a). The heights are offset-corrected so that the floor of each profile is set to zero (gray-dotted line). The colored-dotted lines indicate the average of all data points contributing to their respective higher levels (ME: 27.4 nm, AE: 18.0 nm).

2.3.2. ROOM TEMPERATURE: NP TRAPPING

To test that the devices are properly fabricated, the current vs. voltage (IV) characteristics are recorded, at room temperature, in vacuum. Figure 2.6a shows a false-colored SEM image of a device that illustrates the schematic of the electrical circuit. To obtain the IV characteristics a bias voltage sweep is applied between the AE (in dark blue) and the ME (in light blue) while the current through the gap is measured. The bias voltage sweeps from -200 mV to 200 mV, followed by a sweep from 200 mV to -200 mV. Discarded are the devices whose measured current is larger than the noise floor level (~ 2 pA) within this voltage range. In contrast, the devices that display a flat IV curve (grey line in Fig. 2.6b) are the so-called "working" devices; only these devices will be used for further electrical characterization of nanoparticles (NPs). The local-back gate (GE), covered with HfO_2, is colored in light fuchsia (panel (a)), which is connected to a separate voltage source to perform gating measurements. The GE is not used for the NP-trapping checking. In dark fuchsia (panel (a)) the substrate coated with HfO_2 is indicated.

In this dissertation, the drop-casting method is used for all particle deposition on chips, followed by prompt vacuum pumping. A maximum of three depositions of 2-4 μl was allowed for each chip. The trapping of NPs is confirmed by a clear increase in the measured current. Figure 2.6b shows an example of a device (#11, chip C) that was empty before the deposition (in solid gray dots), that contained trapped NPs after the deposition (in fuchsia). In this particular case, 40 nm Au NPs were trapped after the second deposition, showing an almost linear IV, accompanied by a weak hysteretic behavior when sweeping the voltage up and down.

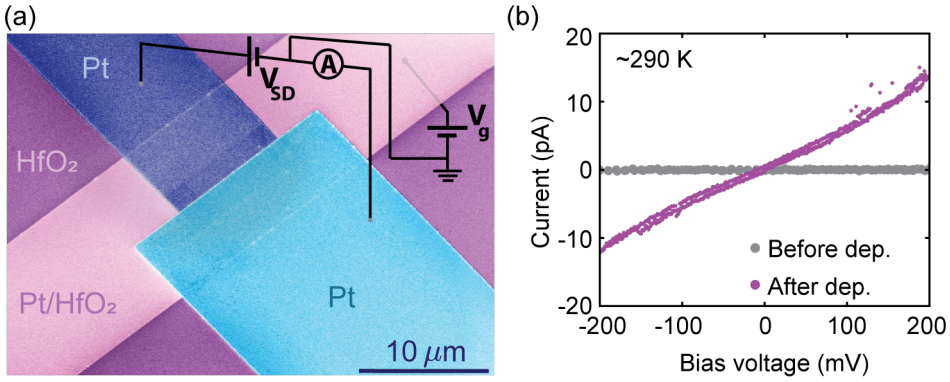

Figure 2.6: (a) Schematic circuit of a wide self-aligned nanogap with a local gate (device #14, chip B), in a false-colored SEM image. AE, in dark blue; ME, in light blue; GE; in light fuchsia; substrate, in dark fuchsia. (b) Electrical characterization of device #11 (chip C) before (solid grey dots) and after (fuchsia dots) 40 nm Au NP deposition, measured at room temperature, in vacuum. The grey dots exhibit an open circuit, indicating a working empty device. The increase in current shown by the fuchsia dots indicates the capture of Au NPs. The current is measured while the voltage is swept up and down between ± 200 mV in a cryogen-free probe station.

Spherical gold NPs with a diameter of 10 (9-11) nm and 40 (37-43) nm were used as reference particles to test our wide self-aligned nanogap devices. These particles are purchased from BBI International, as water-based solutions with citrate as the capping

agent. The catalog numbers are #SKU EM.GC40/7 and #SKU EM.GC10/4, respectively.

In this chapter, chips A, B, and C are fabricated in the same batch, displaying a yield of 2-3 open devices. Chips A and B are used for device inspection (with AFM and SEM). Chip C is used for electrical measurements, in particular, of devices #11 and #14.

2.3.3. LOW TEMPERATURES: *IV* CHARACTERISTICS

After the second deposition of 40 nm Au NPs on chip C, device #11 contained particles (Fig. 2.6b). Device #14 trapped particles after the deposition of 10 nm Au NPs (Appendix, Fig. A2.12), performed after the second deposition of the 40 nm NPs. After each successful trapping, the devices were cooled down below 10 K. In this chapter, all of the low-temperature measurements on device #11 were performed in a cryogen-free probe station, while the measurements on device #14 and its respective NP deposition were performed in a variable temperature insert (VTI). The probe station was replaced with the VTI due to difficulties in connecting the probes to the ME and (or) to the AE at temperatures below 20 K, most likely due to condensation and water freezing of residual moisture on the tips of the probes acquired after the room temperature measurements. A VTI requires wire bonding of the chip to a chip carrier; the latter facilitates the interconnections from the chip to the pins of the VTI, avoiding connection problems at low temperatures.

Figure 2.7a shows the IV measured on device #11, at 9.0 K, which displays a single transport gap centered around zero bias. Panel (b) displays the IV measured on device #14, at 2.0 K, characterized by asymmetric step-like features. Both behaviors are Coulomb blockade-like features; the IVs are stable (no hysteresis), and present a resistance value between 1 and a few tens of GΩ.

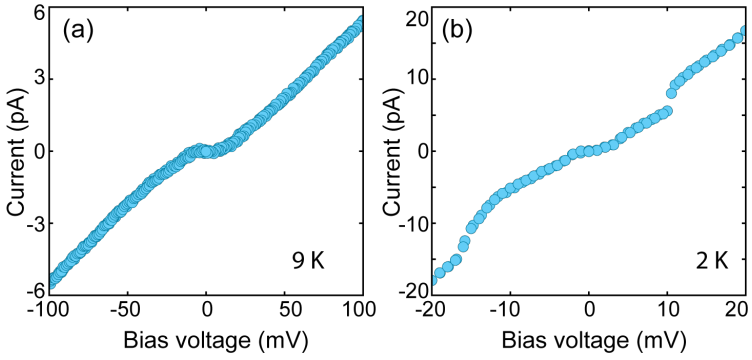

Figure 2.7: Experimental IV characteristics acquired on two different devices of chip C, at low temperatures, measured in a probe station and a variable temperature insert (VTI). The IVs show a single transport gap centered around zero bias (panel (a)) or asymmetric step-like features (panel (b)). (a) IV measured on device #11, at 9.0 K, after 40 nm Au NP deposition, in a probe station, obtained by applying a complete voltage sweep (up and down); Fig. 2.6b shows its room temperature measurement. (b) IV measured on device #14, at 2.0 K, after 10 nm Au NP deposition, in a VTI, obtained by applying a voltage sweep from negative to positive values. The room temperature measurement of this device is shown in the Appendix, Fig. A2.12.

2.3.4. LOW TEMPERATURES: GATING

As stated in the introduction of this chapter, the aim of this study is the generation of single-electron transistors (SET), based on wide self-aligned nanogap devices with a local gate. A SET is a three-terminal device of a conductive island, connected to a source and drain electrodes and capacitively coupled to a (local) gate. The gate coupling (α) is a parameter that indicates the ratio of the gate capacitance (C_G) to the total capacitance ($C = C_1 + C_2 + C_G$). The larger α is (up to 1), the more efficiently the electrochemical potential of the island can be changed compared to those of the electrodes. As a consequence, more charge states can be accessed for large α, and therefore lower gate voltages are required to effectively modulate the charge transport.

Figure 2.8a displays the stability diagram acquired on device #11 (40 nm NP) shown as a colormap of the differential conductance (dI/dV) as a function of the gate voltage (V_G) and source-drain voltage (V_{SD}), at 8.5 K. A Coulomb diamond-like feature is visible, indicated by the white-dotted lines. Panels b, c, and d exhibit three IVs measured at different gate voltages, confirming gate-modulated transport. The slopes of the Coulomb diamond (β, γ) provide information on the gate coupling parameter (α) through the relation $\alpha^{-1} = \beta^{-1} + \gamma^{-1}$, obtaining $\alpha = 0.012$ for this device.

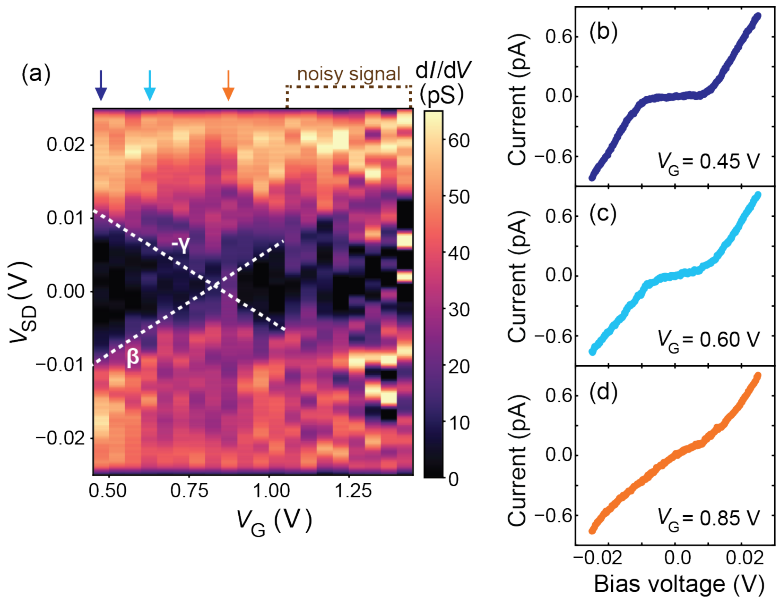

Figure 2.8: (a) Experimental stability diagram acquired on device #11 (chip C) shown as the colormap of the differential conductance (dI/dV) as a function of the gate voltage (V_G) and source-drain voltage (V_{SD}). V_{SD} is swept from negative to positive values, at 8.5 K, after drop-casting 40 nm Au NPs. The white-dotted lines are a guide to the eye indicating the presence of a Coulomb diamond-like feature. From the slopes, $\beta = 0.023$ and $\gamma = 0.023$, we determined the gate coupling (α) to be 0.012. Panels (b),(c), and (d) show individual IV curves measured at a gate voltage of 0.45 V, 0.60 V, and 0.85 V, respectively. The dI/dV of these IVs is indicated with the corresponding colored arrow in panel (a). Note that for this device the IVs were unstable for V_G>1.05 V leading to a "noisy" signal in the dI/dV map.

Another SET was obtained through device #14 (10 nm NP); its stability diagram measured at 1.6 K is shown in Fig. 2.9. The blue numbers (above the graphs) indicate the order in which the stability diagrams were acquired while sweeping V_{SD} from negative to positive values. The blue arrows establish the direction of the sweeping V_G. Panel (a) presents two stability diagrams, recorded consecutively. Close to 0.2 V, an offset charge change occurred which was corrected by placing the two diagrams separately. The light-blue-dotted lines denote Coulomb diamond-like features, including several parallel lines with the same slopes as in the diamonds. Panel (b) exhibits two stability diagrams; on the right side, the same one as the right one of panel (a); on the left side, the consecutively one registered by sweeping V_G from 0.2 V towards negative values. The two diagrams are placed separately to correct for the charge offset change. Again, a clear Coulomb diamond is visible (see red-dotted lines). Remarkably, the same diamond size and slopes are shown in panels a and b, revealing that the gate modulation is reproducible.

The height of the Coulomb diamond equals 4 E_C, with the charging energy defined as $E_C = e^2/2C$, where C is the total capacitance of the NP. Thus, from the diamond indicated by red-dotted lines (Fig. 2.9b), E_C = 5.2 meV and C = 15.4 aF, are obtained. Next, the slopes of the Coulomb diamond (β, γ) relate to the left and right capacitances according to $\beta = C_G/(C_G + C_2)$ and $\gamma = C_G/C_1$, with C_1 the capacitance between the source and the island, and C_2 the capacitance between the drain and the island. Thus, from the red-dotted diamond, C_1 = 7.1 aF and C_2 = 8.2 aF. Finally, from the relation between α and the diamond slopes, α is 0.002.

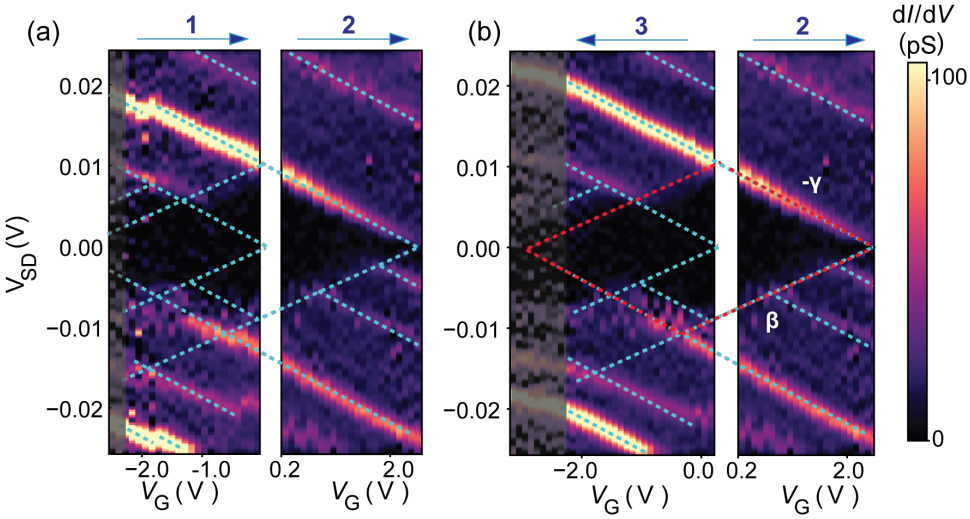

Figure 2.9: Experimental stability diagram acquired on device #14. V_{SD} is swept from negative to positive values, at 1.6 K, after drop-casting 10 nm Au NPs. The blue numbers indicate the order in which the stability diagrams were acquired. The blue arrows establish the direction of the sweeping V_G. (a) Same V_G sweep direction for both diagrams. (b) Different V_G sweep direction for both diagrams. From the slopes and height of the red-dotted diamond, α = 0.002, γ = 0.004, β = 0.003, C_1 = 7.1 aF, C_2 = 8.2 aF, C_G = 0.03 aF. E_C = 5.2 meV.

The total capacitance is consistent with a gold NP of 9-11 nm, compared with the capacitance values calculated from CB fits of particles of similar size (chapter 3, Fig. 3.6) and estimations based on different geometries with similar devices (chapter 3, section 3.4.1). The fact that C_1 is very similar to C_2 indicates that the particle is connected almost symmetrically to both electrodes. However, the gate coupling is rather small compared to the value displayed in device #11. A possible scenario that can account for these values is to consider the gold NP to be placed symmetrically on top of the source and drain electrodes.

Considering all the SETs generated using a local gate, based on gold NPs (this chapter) and ferritin particles (see chapter 4), an average gate coupling (α_{local}) of ~0.06 was obtained (all α values are shown in Table A2.1). In contrast, from the three-terminal measurements performed with the silicon-back gate and ferritin particles (see Appendix, Fig. A2.13), an average gate coupling (α_{Si}) of 0.003 was accomplished. The ratio $\alpha_{\text{local}}/\alpha_{\text{Si}}$ is 23, which indicates an improvement of at least one order of magnitude. To place this value in context, a comparison with reported gate couplings is performed. For this, the data on the gate coupling vs. dielectric thickness is extracted from a calculation in Ref. [16], which considered three-terminal devices with source and drain electrodes. Although these calculations consider a different geometry, dielectric, and metal, the expected $\alpha_{\text{local}}/\alpha_{\text{Si}}$ can be used as a comparator. Figure 2.10 shows the interpolation of the extracted data from that paper considering a gap size of 1.24 nm (light-blue-dotted line) and 2.0 nm (black-dotted line). The red dots indicate the gate coupling for a dielectric thickness of 22 nm, which is approximately the thickness of the dielectric of the local gate in our study. The green dots indicate the gate coupling calculated for a dielectric thickness of 285 nm, which is the thickness of the silicon oxide layer of the substrates. For a gap size of 1.24 nm and 2.0 nm, $\alpha_{\text{local}}/\alpha_{\text{Si}}$ is 14 and 10, respectively, therefore one order of magnitude difference is expected which is consistent with the one-order improvement of the gate coupling that was obtained.

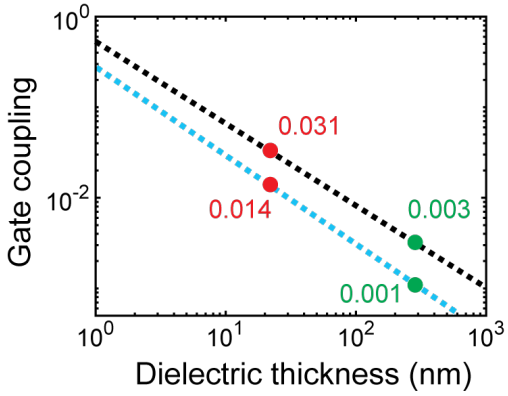

Figure 2.10: Gate coupling (α) as a function of the dielectric thickness, based on the interpolation of the data extracted from [16], with $\epsilon_r = 9$ and a source-drain electrode thickness of 0.6 nm, for a gap size of 1.24 nm (light-blue-dotted line) and 2 nm (black-dotted line). The gate coupling for a dielectric thickness of 22 nm and 285 nm is highlighted with red dots and green dots, respectively. $\alpha_{22\,\text{nm}}/\alpha_{285\,\text{nm}}$ is 14 and 10 for a gap size of 1.24 nm and 2.0 nm, respectively.

After finishing all measurements, SEM inspection was performed on both devices (#11 and #14). Figure 2.11a depicts the SEM image of device #11; a large variation of the gap size is observed (9-50 nm), indicating that a connection of a 40 nm NP to the electrodes is feasible. Figure 2.11b displays the SEM image of device #14; a gap-size range from 4-5 nm to 20 nm is present, therefore, a 10 nm particle could be both, strongly or weakly coupled to the electrodes. This is consistent with the scenario presented for the measurement shown in Fig. 2.9. Additionally, both images show that the NPs can be found individually (encircled in yellow) or aggregated (encircled in green).

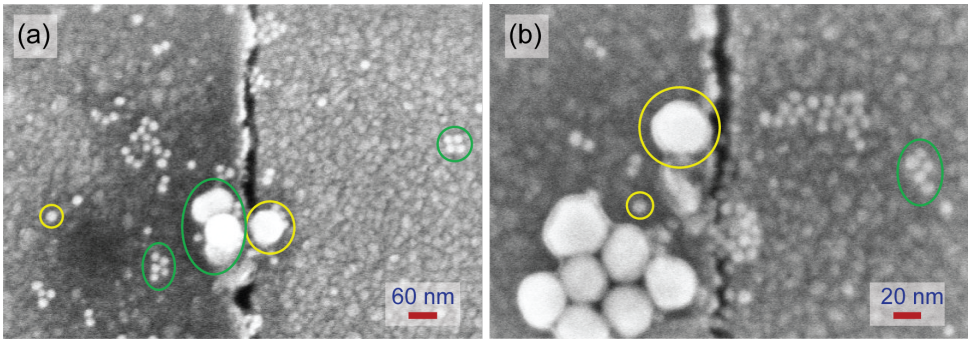

Figure 2.11: Scanning electron microscopic images from device #11 (a) and #14 (b), performed after the measurements were finished. In yellow, individual particles are indicated. In green, NP aggregates are encircled.

2.4. CONCLUSIONS

In this chapter, we have demonstrated our principal goal, which is the fabrication of single electron transistors by trapping nanoparticles in wide self-aligned nanogap devices implemented with a local gate. In particular, we have generated SETs with gold nanoparticles of 10 nm and 40 nm in diameter. For both types of NPs, below 10 K, the resistance was found to be between 1 to tens of GΩ and the IVs were stable and free of hysteresis. At room temperature, the resistances were in the GΩ range as well, indicating that the tunneling resistances are temperature independent, which is expected for a transport dominated by charging effects.

From the perspective of gating performance, the gate coupling of the devices improved by one order of magnitude compared to that of traditional three-terminal devices using the silicon-back gate of a standard silicon substrate. Although a gate coupling of 0.07 is far from 1, it proves that the expected electrode screening of the electric field generated by the wide electrodes can be overcome with the inclusion of a local gate. In future experiments, a reduction of the dielectric thickness could be implemented, which should result in a larger gate coupling. Additionally, since the immersion in the chromium etchant needs to be as brief as possible (less than a minute) to avoid damage to the hafnium oxide dielectric, other dielectrics need to be explored that can tolerate longer times while being immersed in the chromium etching, to reduce variations of the gate coupling for the same particles. Finally, the versatility of the NP trapping process in these devices facilitates the extension of the methodology to generate single-electron transistors based on different nanoparticles, such as metal/oxide-based particles, and bioparticles.

2.5. APPENDIX

2.5.1. CURRENT-VOLTAGE CHARACTERISTICS AT ROOM T

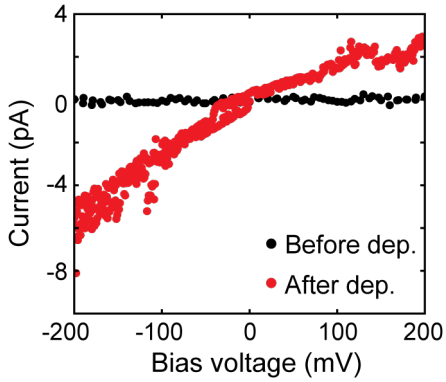

Figure A2.12: Electrical characterization of device #14 (chip C) before (black dots, 9 K) and after (red dots, room temperature) 10 nm Au NP deposition, measured in vacuum. The black dots indicate an open circuit. The increase in current shown by the red curve confirms the capture of Au NPs. For the measurements, the current is measured while the voltage is swept up and down between ± 200 mV. Note: The data before deposition was recorded at 9 K, before the corresponding deposition.

2.5.2. SILICON BACK GATE

Experimental stability diagrams acquired on four different devices (Ft4, Ft5, Ft6, and Ft7), in the same chip, are shown in Fig. A2.13. These three terminal devices used the silicon-back gate of a standard silicon substrate and horse-spleen ferritin NPs (same as the ones used in chapter 3). These devices are self-aligned nanogaps fabricated following published fabrication routes [12, 13].

Table A2.1: Summary of the gate coupling (α) obtained for three-terminal devices using the local-back gate, with both Au NPs and ferritin (Ft) NPs. In addition, also provided are the α values obtained for devices that used the silicon-back gate of a standard silicon substrate, with Ft NPS.

Gate type	Device	α
local (Ft NPs)	Ft 1	0.0089
	Ft 2	0.0106
	Ft3 (s)	0.2943
	Ft3 (b)	0.0286
local (Au NPs)	#11	0.0115
	#14	0.0018
Si-back gate Ft NPs	Ft 4	0.0066
	Ft 5	0.0048
	Ft 6	0.0001
	Ft 7	0.0005

(s): parameters extracted from a small diamond
(b): parameters extracted from a big diamond

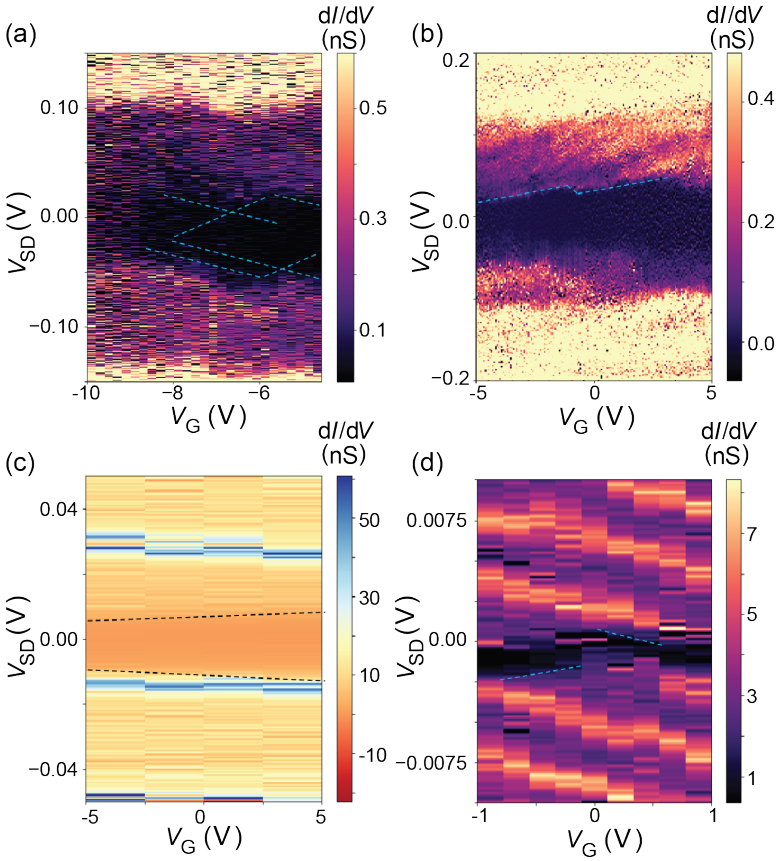

Figure A2.13: Experimental stability diagrams acquired on devices Ft4, Ft5, Ft6, and Ft7, at temperatures below 10 K after particle trapping, using the silicon-back gate and ferritin NPs. V_{SD} is swept from negative to positive values. The dotted lines are a guide to the eye indicating the presence of Coulomb diamond-like features. From the slopes (β and γ), the gate coupling (α) is determined. (a) Device Ft4; $\alpha = 0.0066$, $\gamma = 0.0106$, $\beta = 0.0175$. (b) Device Ft5; $\alpha = 0.0048$, $\gamma = 0.0195$, $\beta = 0.0064$. (c) Device Ft6; $\alpha = 0.0001$, $\gamma = 0.0002$, $\beta = 0.0002$. (d) Device Ft7; $\alpha = 0.00045$, $\gamma = 0.0019$, $\beta = 0.0006$. The average gate coupling is 0.003 .

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