Towards optical detection of a single electron

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5

Single-electron fabrication

In chapter 4 we discussed the role of SETs in single-charge control and trapping. Then we introduced two methods for optical detection of single electrons by using SETs combined with high-resolution spectroscopy on single DBT molecules. It was shown that to use a SET as an electron trap, it must have features that distinguish it from traditional SETs built earlier. The most important aspect is that the electric field created by the charged island should not be screened by any bulk metallic structure. Several fabrication methods were tested to produce favourable SETs for optical charge detection and a fabrication recipe was developed. This chapter describes all the efforts directed at SET fabrication during this PhD work.

A popular method to fabricate SETs is the shadow evaporation technique. [1–6] In this method, the island and electrodes are patterned on a resist with a large undercut (typically a few hundred of nanometre) using lithography, metal deposition and oxidation at different angles, and lift-off. Although shadow evaporation is a well-established technique, the SETs fabricated in this way almost always display an artefact of bulk metal around the main island that would screen the electric field of an electron. It renders this method unfavourable for making SETs for optical charge detection. In the following section, the fabrication processes used in this thesis to fabricate single-electron traps are described in detail. Initially, the fabrication started with e-beam lithography. Later we went through many other techniques such as focused ion beam milling, self-assembly of nanoparticles, and finally, a hybrid method using Atomic Layer Deposition (ALS) combined with e-beam lithography. The detailed description of the equipment used in this project can be found on Leiden University nanolab and Kavli nanolab websites [7,8].

5.1. Electron beam Lithography

In section 4.1.3, it was demonstrated that the charging energy condition can be easily satisfied with an island of 100-300 nanometers at 1.5 Kelvin. This resolution is within reach of conventional electron-beam (e-beam) lithography.[7] In general, creating patterns using e-beam lithography relies on 4 main steps, namely: coating with an e-beam-sensitive resist, e-beam pattern generation, development of the exposed parts of the resist and descum (cleaning of residual resist after development). Those steps are shown in Figure 5.1.

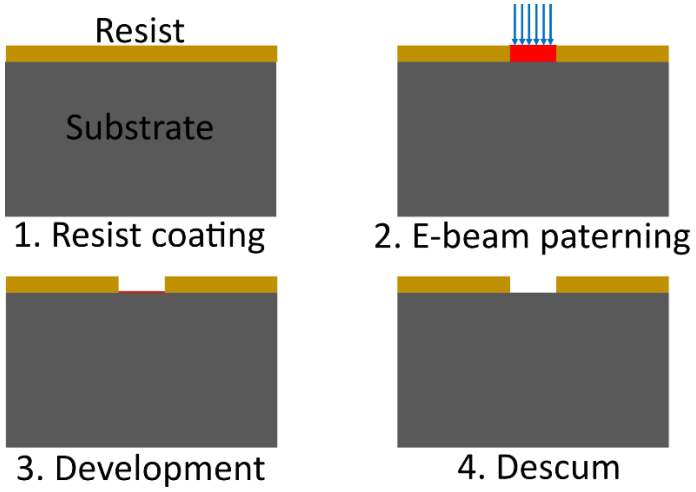

Figure 5.1: 4 main steps of e-beam lithography consisting of resist coating, electron beam exposure, developing and descum.

5.1.1. Substrate preparation

All the fabrication in this thesis has been done on silicon (100) wafers supplied by University wafer. This substrate surface had 300 nm wet thermal silicon oxide on the polished side. Such an oxide layer is sufficient to avoid any current leak to the substrate. A diamond cutter was used to cut silicon wafers into squares of 1×1 cm^2. The substrates were then flushed with isopropanol and blow-dried with a nitrogen jet to remove silicon grains left from cutting. Then the substrate was stored in boxes with sticky bottom to prevents scratches and damage.

5.1.2. Resist coating

After lithography and during metal deposition, there is always some material stuck in sharp corners and against vertical PMMA walls. This normally causes difficulties in lift-off and the formation of 'flaps' at the edges of structures (Figure 5.2.a). Bi-layers or multilayers are needed for producing undercut patterns to avoid flap formation and to increase patterning resolution. [9–12] A good undercut pattern consists of at least two layers of resists with different sensitivity. The more sensitive layer is placed between the substrate and the patterned layer (Figure 5.6.b). As a result, during lithography, this layer is overdosed and creates an empty space between the substrate and the pattern. Figure 5.6.a and b show the difference between having and not having an undercut layer. As can be seen, a bilayer undercut produces edges with much better quality and without any flaps.

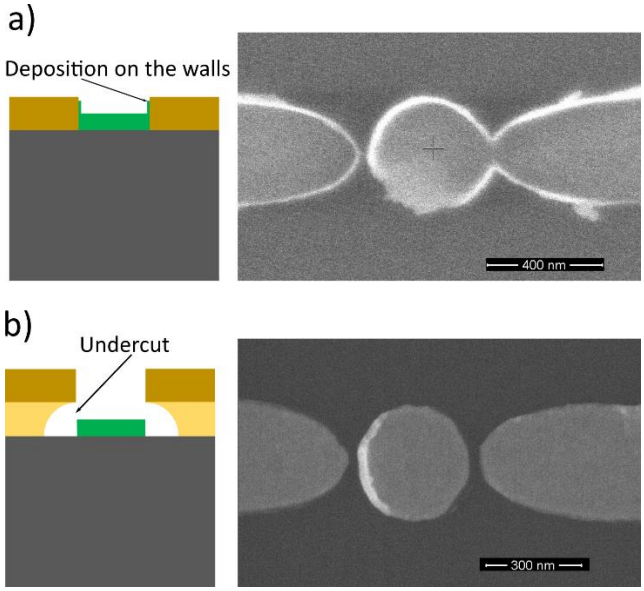

Figure 5.2: a) Use of single-layer resist causes flap formation because metal deposition on the walls whereas a bilayer resist b) creates a cavity or undercut between the substrate and the patterning resist that prevents flap formation and produces smooth edges.

The following steps are performed for the resist coating. To create the undercut we have chosen an e-beam-sensitive resist consisting of a double-layer stack out of PMMA 662.06 (600 kDa) and PMMA 672.045 (950 kDa) from ALLRESIST both are positive resists. The following protocol was used to coat the substrate with the resist:

1. Sonicating the substrates in an acetone bath for 2 minutes.
2. Taking the substrate out and immediately flushing with synthesis grade iso-propanol before acetone dries.
3. Blow-drying with nitrogen jet.
4. Mounting the substrate onto the spin-coater using vacuum. Drop-casting PMMA on the substrate with a clean pipet. After transferring the PMMA to the pipet it is better to push the liquid a little bit back into the bottle to avoid bubbles. It is very important to use a small droplet just enough to cover the surface of the substrate. Extra PMMA flows underneath the substrate and causes the sample to tilt on the e-beam stage. The result of this tilt is a change in the focus of the beam and a loss in resolution.

5. Spin-coating of the resist. Start with a spreading step of 1-4 second at 500 rpm followed by 1 minute at 4000 rpm.
6. Baking the resist on a hot plate for 2 minutes at 180°C.

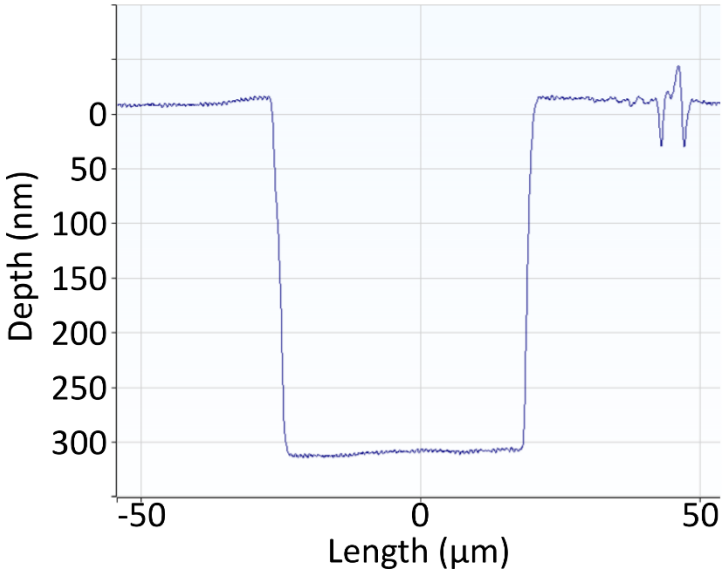

Figure 5.3: profilometry measurement of the thickness of PMMA 662.06 (600k) spin coated at 4000 rpm, 60 s and baked for 2 minutes at 180 °C.

First, the PMMA 662.06 was coated on the substrate then PMMA 672.045 was added. Figure 5.3 shows the profilometry data over a cross section of a scratch on coated PMMA 662.06. The 300 nm thickness is in good agreement with the value indicated in the resist datasheet. The thickness of the second layer is 220 nm. The shallow protrusion at the edges is due to the shrinkage of the polymer during scratching.

5.1.3. E-beam pattern generator

The electron beam pattern generator EBPG Raith-100 was used. The E-line software was used to design the structures. A small scratch was made in one corner of the substrate before placing it on the device stage (Figure 5.4). This scratch is to define the origin of coordinates and to find it in case of second lithography patterning on the same sample. Also, particles produced during scratching are used as a reference for better e-beam focusing (by making sharp images of those).

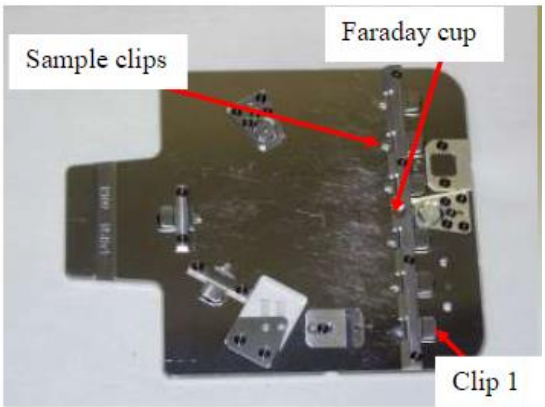

Figure 5.4: Sample stage of Raith-100 with 6 different sample clamps with a Faraday cup to measure current and clips to hold the substrate.

The electron exposure using EBPG Raith-100 has several parameters that must be optimized to achieve the best resolution. They are beam-step size, beam diameter, beam current, acceleration voltage and exposure dose. There is a clear link between the resolution and all these parameters, but most of them except for the dose are machine-specific. The optimal exposure dose varies depending on the resist type, shape, and size of the structures. Therefore, it is necessary to perform dose tests. A good starting point for PMMA 672.045, which is the patterning resist here, is 300 $\mu C/cm^2$. After a few rounds of dose test, it was determined that the best dose for writing islands with a radius of 200nm is 260 $\mu C/cm^2$.

In the section 4.1.4 we showed that tunnelling barriers need to be around 1-3 nanometre to have electrically controllable SETs. This resolution goes far beyond the default resolution of e-beam lithography (10-20 nm). However, we tried to break through this limit by using pattern displacement [13] and overdosing. In short, the structures of islands and two electrode tips were repeated many times in an array. Each element of the matrix was slightly different in the dose and the electrode tips position (Figure 5.5.a). The displacements and doses were distributed according to the initial dose tests to cover all possible gaps between electrodes and the islands. Therefore, the desired gap was expected to be formed at least in one of the structures. However, due to the random displacement errors of the beam, the resolution limits of the resist, and the requirement to place two electrodes at the same distance to the island, we could never achieve such a gap in a one-step lithography process. The electrodes were always either touching the island (Figure 5.5.b) or placed too far from it (Figure 5.5.c).

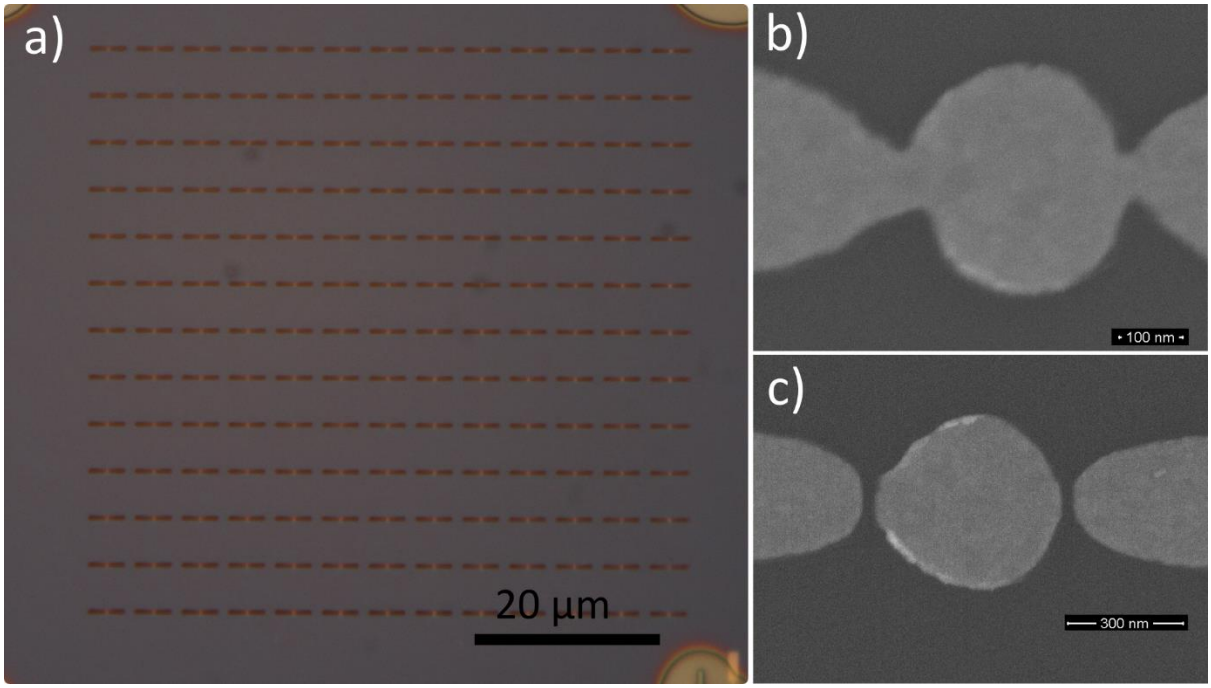

Figure 5.5: a) The design of island with shifted electrode tips. The structure is repeated in an array and each copy has different displacement and dose. b) overdosed sample. c) very big gap 20nm.

5.1.4. Development, descum and metal deposition

Samples were developed in methyl-isobutyl-ketone (MIBK): isopropanol (IPA) mixture (1:3 volume/volume) solution at 25°C for 30 seconds immediately followed by flushing with isopropanol. Dry nitrogen jet was used to blow dry sample after development.

To remove all residual PMMA resist in the trenches descum was applied to the sample. During this process, the left-over PMMA are burned out by oxygen plasma. Descum has a significant effect on the surface quality of the deposited layer.[14]

We used e-beam and thermal evaporation systems to deposit metals on the substrate. Pure gold was used to make nanostructures and to increase the adhesion of gold to the substrate (silicon oxide), 2nm Chromium was deposited first then gold with desire thickness was added .[15,16]

lift-off: In nanofabrication, lift-off is a very tricky and important step. In our structure, the most sensitive parts are the tips of electrodes. The tips of the electrodes are very sharp (few nanometers at the tip diameter). This is to have less electric field shielding by electrodes. The sharp tips are very fragile therefore lift-off process must be very smooth. A recopies was developed to have a very clean and safe lift-off without any metal residual.

- The samples were placed in a large beaker containing 100 ml Acetone. A magnetic stirrer was placed inside the beaker and the lid was properly sealed. And placed on the heater.
- The beaker was heated to 40° C while stirring at 200 rpm for 24 hours. Acetone dissolves PMMA and motion flow created by stirring, peels off the gold layer. The size of the beaker permitted for the stirrer to be at a safe distance from the sample
- To ensure the lift-off is done properly, the sample was checked by optical microscope without removing it from acetone bath. Because PMMA is completely dissolved, any remained gold flake sticks to the substrate if acetone dries. The Van Der Waals force is so strong that removing the attached gold flake is impossible considering that any harsh action like sonication damages the sample.
- Remained unwanted gold was removed by flushing the sample with acetone jet while the sample is still inside the acetone bath.

5.2. Self-assembly

An alternative way to make SETs is to use self-assembly of gold nanoparticles (NPs) and nanorods (NRs). Formerly, Prof Wilfred Van der Wiel and his colleagues at U. Twente showed that it is possible to grab a NP in between two NRs and to define a tunnelling barrier between those (Figure 5.6). Here the NP is the electron box, and the NRs are used as electrodes to deliver electrons to it (source & drain). [14] The main advantage of this technique is that small NPs (tens of nm) can be used to form an NR-NP-NR configuration. As a result, the charging energy is around 10 meV, which is much higher than the thermal energy at 1.2 K, the temperature we can reach in our cryostat.

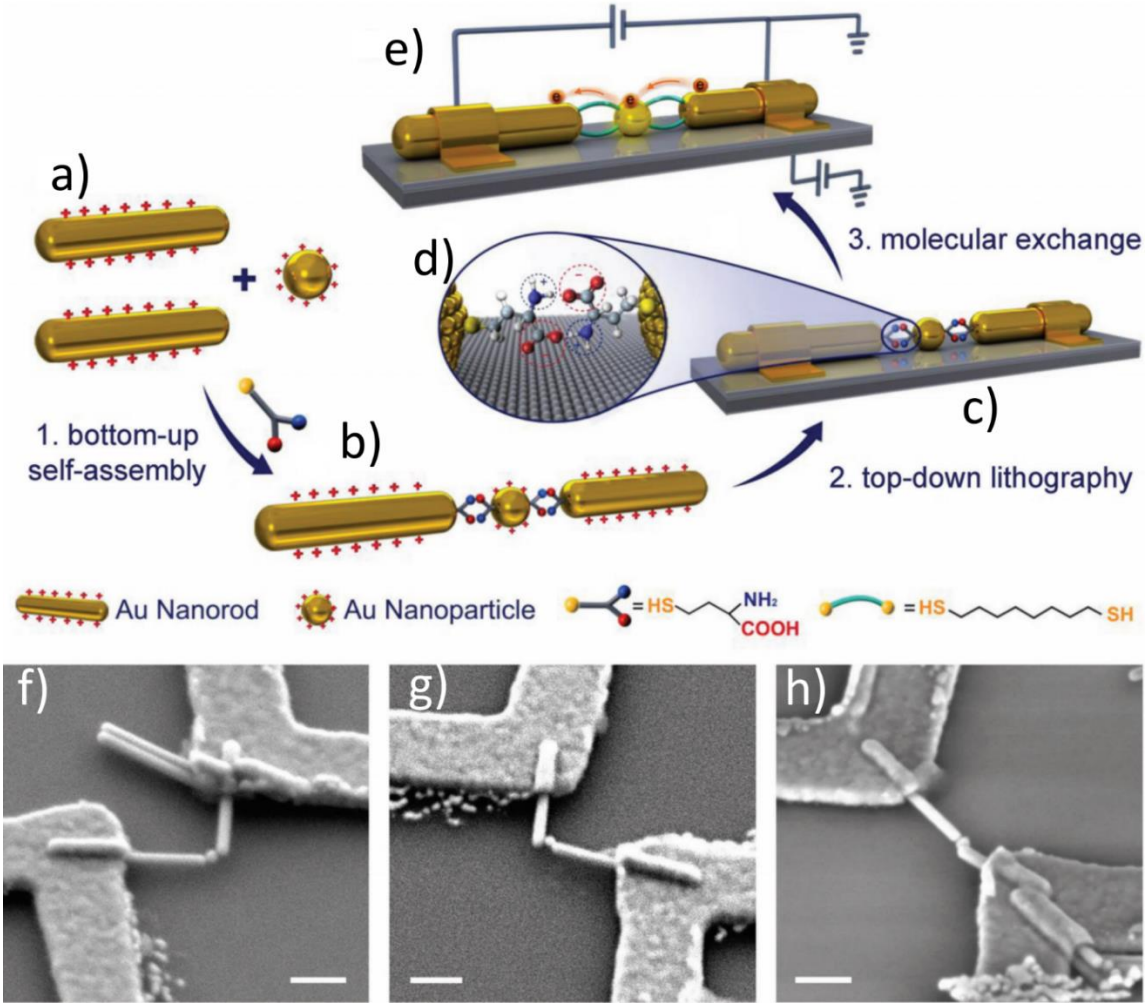

Figure 5.6: Process of bottom-up single-electron transistor fabrication based on the self-assembly of NR-NP-NR particles. a) Two Au NRs and a single Au NP (b) self-assembled as NR-NP-NR linked with homocysteine molecules (c) deposition of the assembly on a silicon substrate in order to form a SET and contacting of the assembly with metal electrodes defined by e-beam lithography. d) Final product by an exchange of the linker molecule homocysteine by 1,8-octanedithiol and. f–h) SEM images of representative SETs; the scale bars correspond to 100 nm. [14]

Homocysteine has been used as an electrostatic linker molecule between the NP and NRs (Figure 5.5.d). The thiol group of the homocysteine binds to the surface of the Au NPs and the tips of the NRs. The zwitterionic groups at the NPs and the tips of the NRs attract each other through a two-point electrostatic interaction and NR-NP-NR assemblies take shape (Figure 5.5.b). Similar to what has been done in [14] the following recipe was used to replicate the NR-NP-NR assemblies:

1. 200 µL of 30 nm gold NPs supplied by Vendor company were added to 800 µL 25 × 10^{-3} m CTAB aqueous solution under ultrasonication. The solution was condensed to 200 µL by centrifugation at 10,000 rpm followed by removal of 800 µL of transparent supernatant.
2. 200 µL of the Au NR solution (40 × 150 nm) was added to 800 µL 25 × 10^{-3} m CTAB under ultrasonication. Then it was centrifuged at 6000 rpm for 6 min, and 960 µL of the transparent supernatant was removed followed by the addition of 160 µL of Milli-Q water.

3. 2 µL of 1×10^{-3} m homocysteine solution and 2 µL of Au NPs solution were added to the NR vial.
4. After 24 hours the solution was drop-casted on a silicon substrate. Note that in the work in reference 14, 120 minutes for the formation of NR-NP-NR assemblies is mentioned. But we did not observe any assemblies after 120 minutes.
5. The substrate was dried with a nitrogen jet.

In scanning electron microscopy (SEM) imaging, different combinations of NP-NR assemblies were observed. As can be seen in the images of figure 5.6, in addition to the desired NR-NP-NR (figure 5.7.a), other assemblies like necklace of NRs (figure 5.7.b) and NP-NR-NP (figure 5.7.c) are also formed.

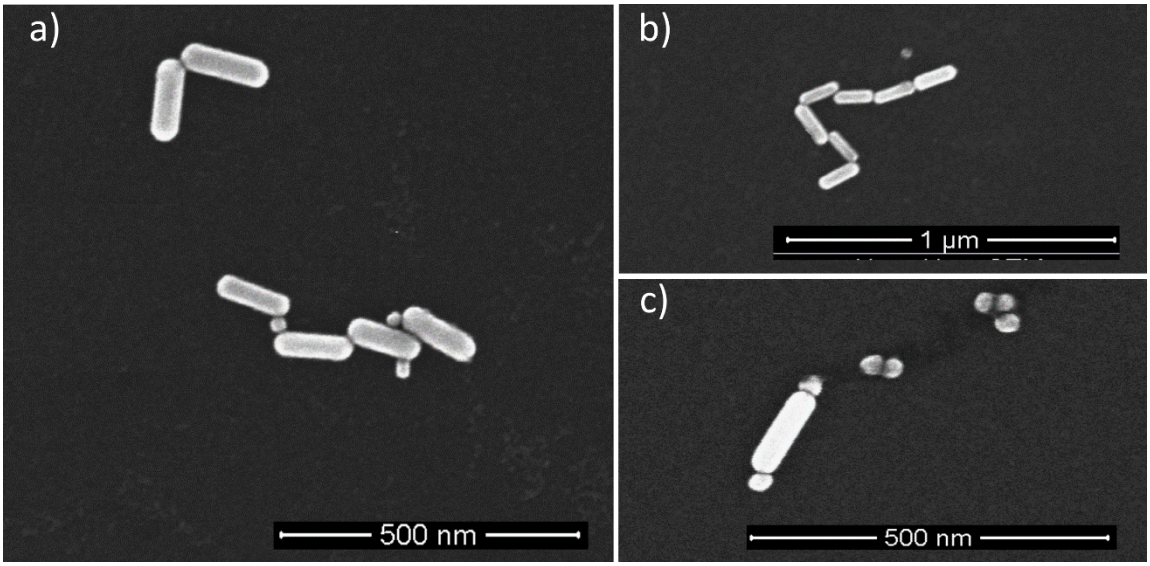

Figure 5.7: a) Self-assembly of the desired combination of a) NR-NP-NR and also other combinations of (b) necklace of NRs and c) NP-NR-NP

The next step in making SETs is to transfer the assemblies to find the desired assemblies on the substrate and connect them to the contact pad. Unfortunately, the clean-room facilities of the Leiden University would not permit the later steps of this fabrication, which prevented us from continuing our work on this project. However, until the time of writing this thesis, we kept on collaborating with Professor van de Wiel's group to proceed with this approach.

5.3. Hybrid recipe to make SETs

In section 5.1 we showed that single-step e-beam lithography alone is not appropriate for making the barriers. However, it is possible to define the barrier by using e-beam lithography along with oxide deposition.[15] Generally, this method consists of three main steps. First, the islands are written on a substrate. Then, they are covered with a layer of insulator (Aluminium or Silicon oxide). Finally, the electrodes are added in such a way that they slightly overlap with the island. The oxide layer isolates the islands, defines the tunnelling barrier, and at the same time simplifies the alignment of the contacts to the island. Figure 5.8 shows the overall process. The main challenge of this approach is to accurately define the thickness of the insulator layer.

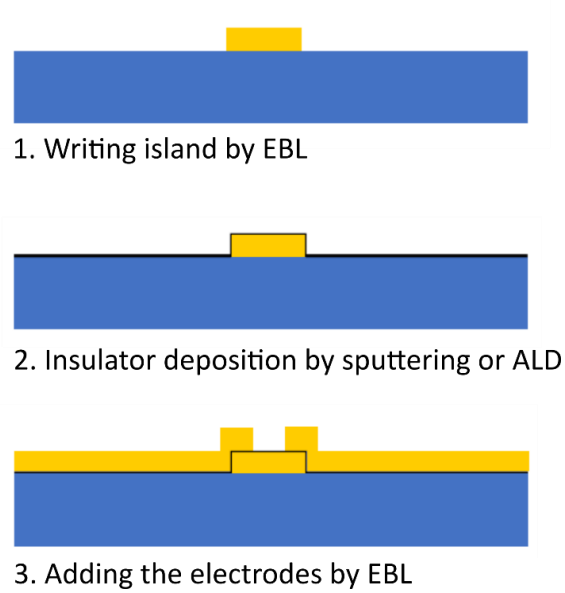

Figure 5.8: General overview of the hybrid method consisting of 3 main processes: 1. Patterning the island by EBL. 2. Covering the island with an insulator layer such as SiO_2 or Al_2O_3 by sputtering or ALD. 3. Patterning the electrodes.

One way is the deposition of thin films on the surfaces by sputtering. During sputtering a source material (target) is bombarded with accelerated ions. The energetic ions tear off target atoms or molecules as either individual atoms or clusters of atoms or molecules. The ejected particles land on the surface of the sample and coat it with a thin film. The thickness distribution of the coated films depends on the angular distribution of sputtered particles, on the collisions between sputtered particles and gas molecules, and on the shape of the target. [16] Because of the particles' collisions and scattering, the coated layer covers both vertical and horizontal surfaces. The ratio between horizontal and vertical deposition strongly depends on the distance between the sample and the target. [16] For the sputtering device available at Leiden university [7] this ratio is measured to about 30% for silicon oxide. Therefore, in order to achieve a tunnelling barrier of 1 to 3 nanometre on sides of the disk shape islands, a silicon oxide layer of 4 to 10 nanometre is needed.

Electrical measurements showed that sputtering is not a reliable method in making barriers. The non-uniformity of the sputtered film in thin layers causes either short cuts or excessive resistivity in the samples. Another disadvantage of sputtering is the instability of the sputtering rate. It makes optimizing the coated layer almost impossible. Also, silicon oxide in thin film is not a good insulator and often causes leakage due to pinholes. [17] Therefore, we abandoned the approach of sputtering silicon oxide and sputtering and considered alternative methods with more precise control over the thickness.

5.3.1. Atomic Layer Deposition

Atomic layer deposition (ALD) is a technique for thin film deposition with atomic precision control over the thickness. The process of ALD is based on vapor chemical process in which a thin film grows layer by layer. Each layer consists of a two-dimensional layer of single atoms or molecules. In each individual layer the substrate is exposed to a pulse of precursors molecules in vapor shape. The precursor molecules react on the surface of the substrate in a self-limit manner. The reaction stops as soon as all the reaction sites on the surface are full.

Therefore, a single atomic size layer with no overlap forms. A thin film can be grown by repeating the reaction process. In addition to the uniform film over whole sample surfaces, ALD provides precise control over the thickness (atomic size). ALD has been used to deposit many materials [21] and has found wide variety of applications in research and industries. These unique features suggest ALD as an excellent method to make the barrier.

Unlike silicon oxide, aluminium oxide provides better electric insulation in thin layers. It is hard and stable with good adhesion to many surfaces. Also, it has high electrical resistivity ($\sim 10^{-16} \Omega$) and small dielectric constant in thin film (around 3 for a few nanometre). This makes it suitable for barrier fabrication. Al_2O_3 has been used previously as tunnelling barrier in [1-5]. We used ALD to coat the fabricated island and to create a tunnelling junction between the electrodes and the island.

A common reaction for aluminium oxide deposition by ALD is based on the following chemical vapor deposition (CVD) reaction [20].

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4$$

In ALD this reaction is performed in two half-reactions. [20–24]

$$Al - OH^* + Al(CH_3)_3 \rightarrow Al - O - Al(CH_3)_2{}^* + CH_4$$

$$Al - CH_3{}^* + H_2O \rightarrow Al - OH^* + CH_4$$

To deposit Al_2O_3, at first, a sample is exposed to trimethylaluminum (TMA), which would react with hydroxyl groups on the surface. This reaction proceeds until all the surface reaction sites are full. Subsequently, TMA is pumped away. The same process is then performed with H_2O. The H_2O reacts with methyl groups on the surface until this surface reaction reaches completion. [22] The time for each cycle is around 12 seconds and the thickness of each layer is about 1 Å. These cycles are repeated to achieve the desired film thickness.

To deposit Al_2O_3 we used the Oxford ALD device of the Kavli lab at TUDelft. The device can operate at different temperatures from 20 to 500 °C. It has been shown that gold nanostructures at high temperatures deform and even can penetrate the substrate. [25] To avoid any possible damage to the sample, the device was operated at 105°C. Al_2O_3 was deposited on several samples, each with a different number of cycles. Each batch of samples loaded into the ALD machine was accompanied by a bare silicon substrate as a control. This piece was used to measure the thickness of the coated layer using the ellipsometry technique. Based on the ellipsometry data the deposition rate is estimated to about 0.6 Å per cycle. A larger error of around 2 Å has been observed for the first 10-12 cycles due to the measurement errors in a very thin film, or alternatively because of the inhomogeneities in concentrations of the precursors during the first cycles of the deposition. Figure 5.9 shows the thickness of the deposited layer as a function of the number of cycles.

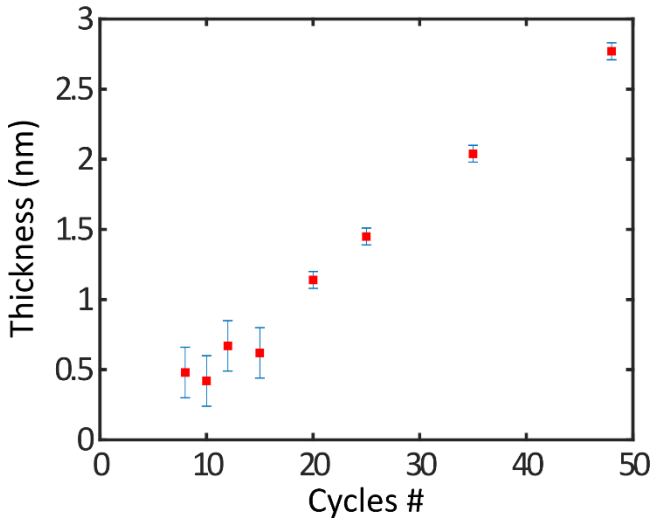

Figure 5.9: Thickness of Al_2O_3 for versus ALD number of cycles measured by ellipsometry.

5.3.2. Final recipe for making SETs

Finally, we have settled on a 10-step hybrid fabrication method that yielded the desired SETs. This method consists of e-beam lithography, gold deposition and ALD. The E-line software was used to draw the structures. Each component is defined in a different layer, allowing us to print them in separate steps. To find writing parameters (dose, beam spot size and beam speed) for the layers, many different tests have been performed. The most critical part of the design is the electrode overlap with island, after 9 round of lithography each round on a chip with 450 SETs, the best shift for the electrodes in respect to the island and the proper dose was found.

In a nutshell, the fabrication recipe consists of 3 lithography steps to pattern the island, make the electrodes, and finally connect these electrodes to the contact pad. Atomic layer deposition was used to insulate the island and to create the tunnelling junction. The final protocol was executed in sequential steps as follows.

1. E-beam lithography to fabricate the islands:
    - Two layers of PMMA resist (662.06-600k and 672.045-950k) were spin coated on the substrates as explained in section (5.1.2).
    - A matrix of 15×15 individual 200 nm islands separated by 5 μm from each other were patterned by Raith-100 e-beam lithography. The islands were written with a beam spot size of 32 nm (PC 14) and a dose of 220 μC/cm.
    - In order to find the structures back during the second and the third steps of lithography, e-beam markers were also patterned in this stage. The suitable dose to write a marker was 360 μC/cm, which provided a beam spot size of 32 nm.
    - Samples were developed in mixture of methyl-isobutyl-ketone (MIBK) and isopropanol (IPA) (1:3 volume/volume) at 25°C for 30 seconds, immediately followed by flushing with isopropanol.
2. Deposition: 2 nm of Chromium and 20 nm of gold were deposited by a resistance evaporator.
3. Lift-off: was done based on the recipe described in section 5.1.4. Figure 5.10 shows one of the fabricated islands with a diameter of about 200 nm.

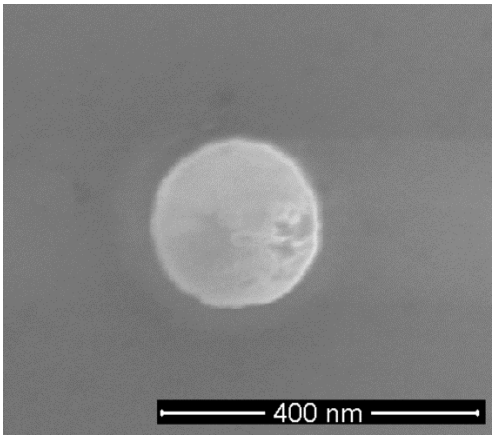

Figure 5.10: 200 nm gold island patterned by e-beam lithography and deposited by the resistance evaporator technique.

4. Insulation: ALD was used to deposit Al_2O_3 with various thicknesses (from 0.6 to 4.2 nm) to electrically insulate the islands.
5. E-beam lithography to fabricate the electrodes: Raith-100 EBPG has an alignment error of up to 50 nm in overlapping two layers printed in two different steps. Previously, it was mentioned that many islands were printed in a matrix. For each element of this matrix the electrodes were displaced with respect to the center of the islands. Repeating this displacement in all directions allowed us to compensate for the alignment error and end up having several perfect structures somewhere in the array. Moreover, to select for the optimal dose, the dose was also varied up to twice bigger than the original value. This would increase the chance of getting the desired overlap between tips of electrodes and island. The procedure for making source and drain electrodes was therefore very similar to the one used for fabricating the islands:
    - Two layers of PMMA resist (662.06-600k and 672.045-950k) were spin coated on the substrates.
    - The electrodes were patterned with a beam spot size of 89 nm (PC 10) and a basic dose of 300 μC/cm.
    - Samples were developed in MIBK:IPA 1:3 mixture at 25°C for 30 seconds immediately followed by flushing with isopropanol.
6. Gold deposition: Initially, 25 nm of gold were deposited at this stage. Later, we found that electrode tips often crack at their overlaps with the island (Figure 5.11). A possible explanation is the height difference between the island and the substrate. This difference creates a shadow during evaporation in case the sample is slightly tilted. As a result, the electrode at the edge of the island disconnects or is thinner and can easily break. To avoid this problem, we found it better to deposit a thicker second layer, with a thickness of at least 1.5 times that of the first layer. At the end, 2 nm Chromium followed by 30 nm of gold were deposited on the substrate.

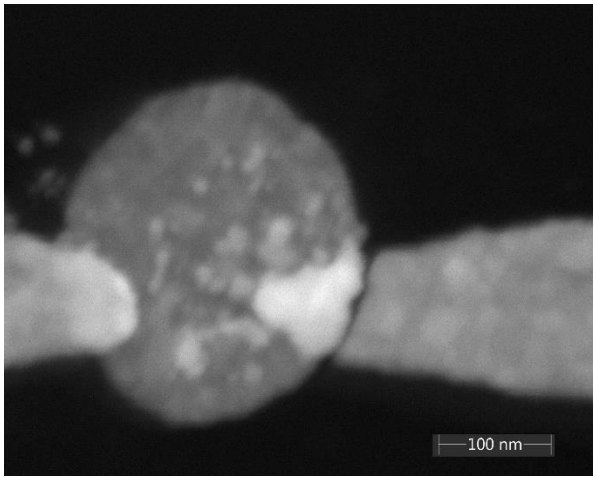

Figure 5.11: A crack in the tip of an electrode caused by insufficient electrode thickness.

7. An SEM (Thermo Fisher Scientific Apreo 2) was used to image the samples and to measure the intersection to calculate the C_S and C_D capacitances. The charging energy depends on this intersection area. Larger intersection areas increase the total capacitance and consequently decrease the charging energy. Considering this limitation and the self-capacitance of the island, the total capacitance of C_S and C_D should not exceed 100 aF. SEM imaging is known to be destructive to the inspected samples due to charging and carbon contamination deposited on the sample. To mitigate these effects the sample was plasma cleaned before inserting it into the SEM and each batch of SETs had an extra twin set to be used for imaging. Figure 5.12.a, b, and c show three examples of fabricated SETs with the desired overlap, a too large overlap, and no overlap, respectively.

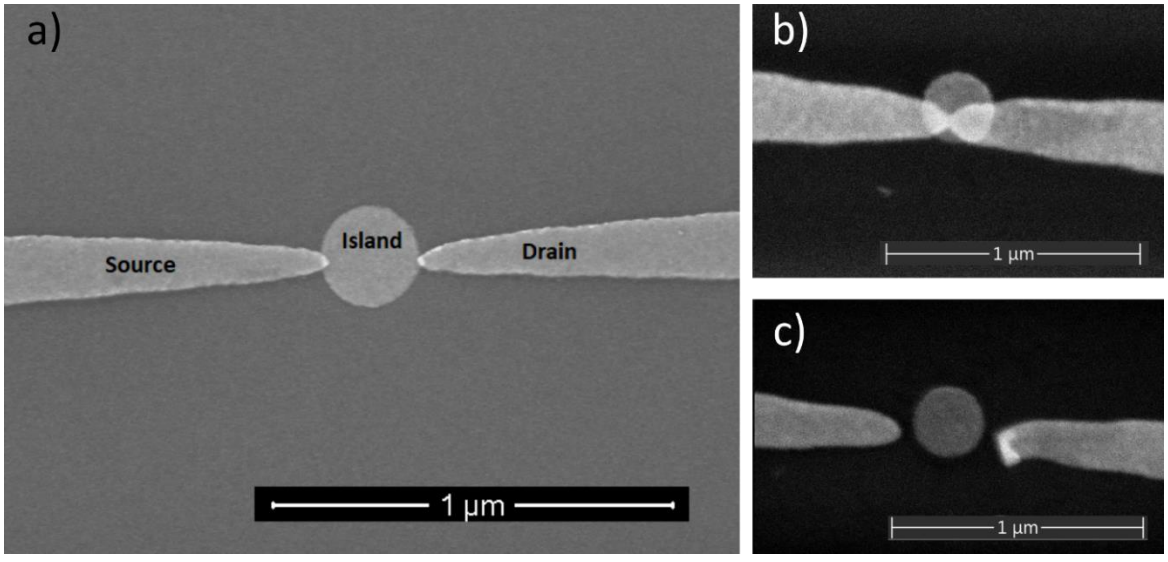

Figure 5.12: Fabricated SETs with different doses and shifts for the electrodes. a) desired intersection between island and electrodes, less than 800 nm^2, resulting in C_S+C_D less than 100 aF. b) over-exposed sample with a too large overlap and short contact between electrodes. c) no overlap.

8. E-beam lithography was used to connect well-fabricated SETs to 200×200 μm^2 contact pads using a dose of 280 µC/cm and a beam spot size of 800 nm (PC 1).
9. 2 nm of Chromium were deposited as adhesion layer followed by 50 nm gold using the resistance evaporation technique. The contact pads were chosen to be thicker because

during wire bonding, the wire penetrates at least 30nm into the pad. The extra thickness is needed to prevent the wire from reaching the silicon and leaking current to the silicon substrate.

10. Lift-off was done based on the recipe described in section 5.1.4. Figure 5.13 shows the final product.

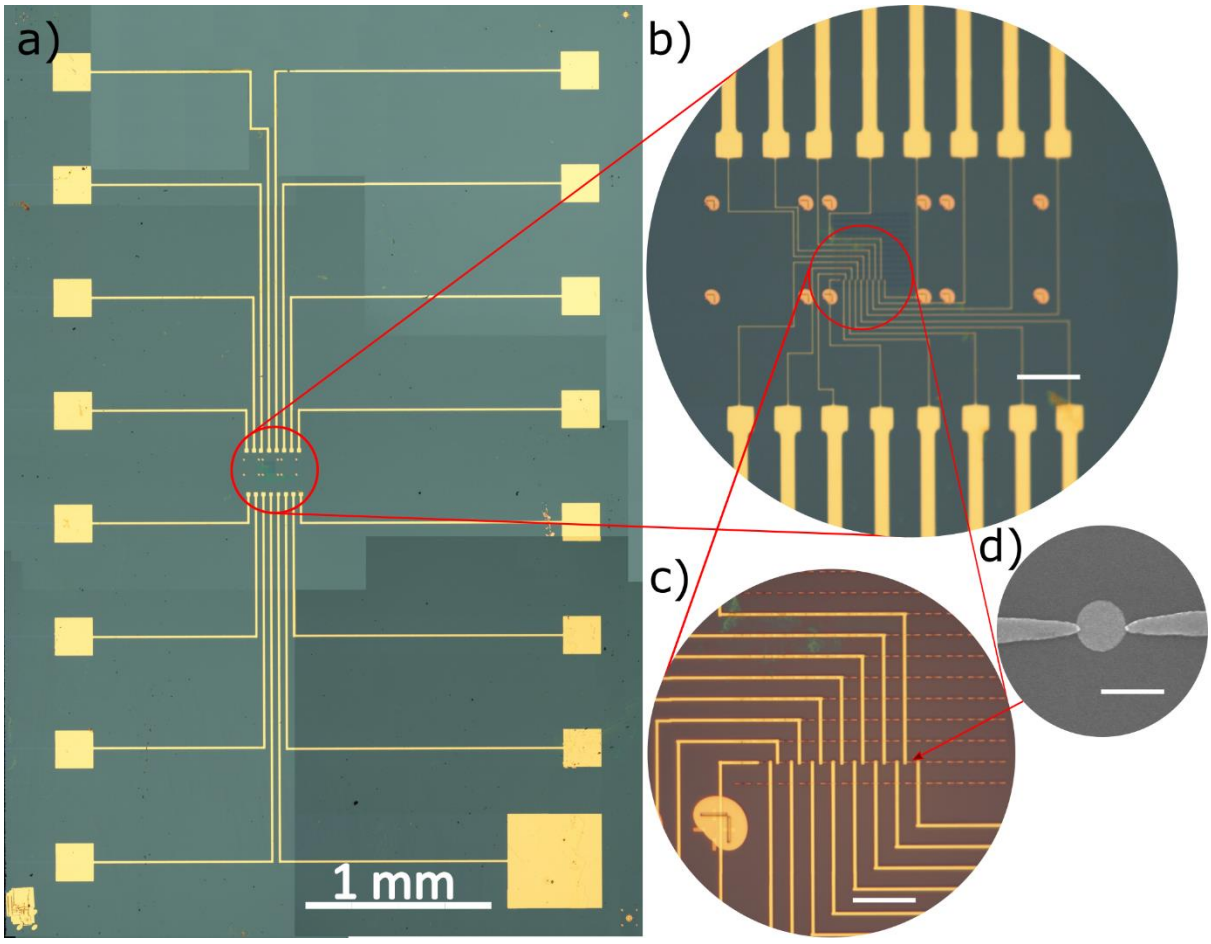

Figure 5.13: Final product of our hybrid recipe to fabricate SETs. a) An overview of the fabricated electronic chip with 16 contact pads to connect 8 SETs. b) A 20 times zoom-in image to the region that the big contact pads connect to the microstructures, scale bar 50 µm. c) A 100 times zoom-in to the region that SETs are located and the SETs are connected to the bigger structure with 500 nm width leads, scale bar 10 µm. d) An SEM image of desire SET, scale bar 250 nm.

5.4. Sample storage and transport

Since the SET samples rely entirely on tiny nm-sized gaps between the electrodes and the island, they are prone to disastrous damage through dielectric breakdown. Therefore, these samples are extremely sensitive to stray electrostatic charges.

In order to reduce the risk of damage, the following protocol was always carefully followed, as a single mistake can ruin days of work:

- Samples were coated with Electra92 (Allresist) conductive polymer immediately after the final lift-off. Electra 92 resistivity is 1Ω/m. it creates a parallel circuit to the transistors with much less resistivity. This parallel circuit

makes equal electric potential between any two points of the sample and transfers incident stray charges safely.

- We always wore a wrist strap connected to the ground while working with the sample.
- Any unnecessary insulators were removed from the working desk.
- Extreme care was taken to avoid any contact with the chip leads.
- The sample was kept in a box with a sticky bottom to prevent it from moving around.
- The sample box was sealed with a static shielding bag during transportation.

Despite all these precautions, many samples were damaged during transportation or preparation. Figure 5.14 shows some examples of these damages. It is almost impossible to know when and how the damages occurred. The only reliable solution is taking absolute care during sample transportation and preparation.

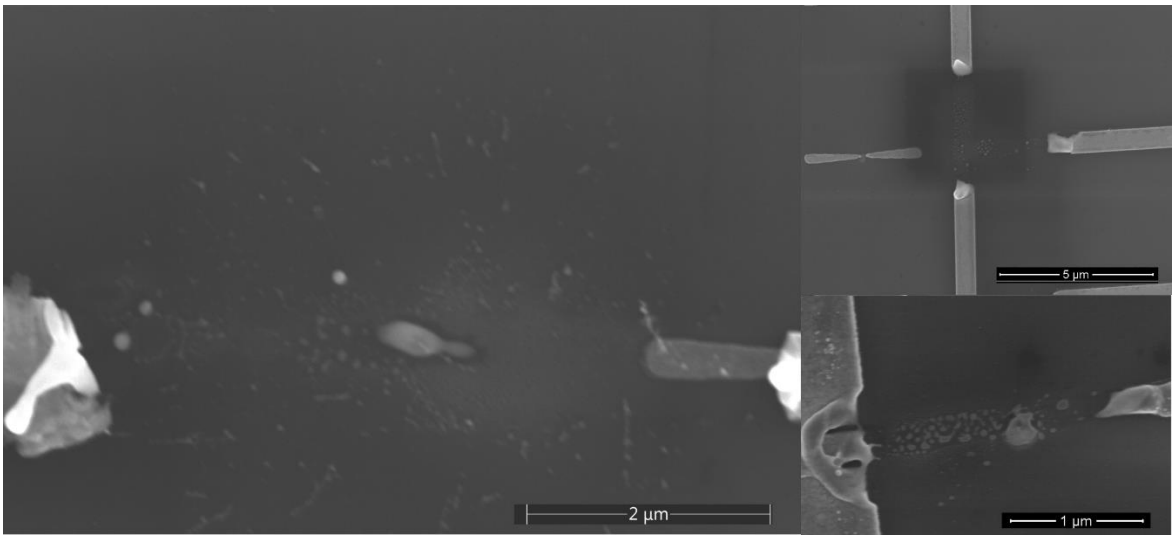

Figure 5.14: Some examples of samples damaged by static electricity.

5.5. Electrical measurements

At the early stages of the project, the electrical measurements were done in Leiden. The sample was wire-bonded to a printed circuit board and attached to the cryostat insert. The cryostat used for electrical measurement is an Oxford instrument Teslatron closed-cycle cryostat that was purchased by the Leiden University condensed matter section within the Nanofront program. Then current-voltage measurements were acquired by the Keithley source-meter model 2450SMU. The measured I-V characteristics, unfortunately, did not display the expected behaviour for SETs, due to damage or to current leakage. Later, SEM images revealed that all measured samples at this stage were damaged. The tip of the electrodes melted in all SETs and the tunnelling barrier was destroyed. SEM images of the sample taken after each step from preparation to measurement revealed that the samples were damaged during the measurement. Figure 5.15 presents some of the damaged samples. To overcome this problem, the set-up was refurbished so that the risk of damaging the sample was minimized. The electrical measurements have been performing at Leiden University and Delft University of Technology with collaboration with Prof. Herre Van der Zant.

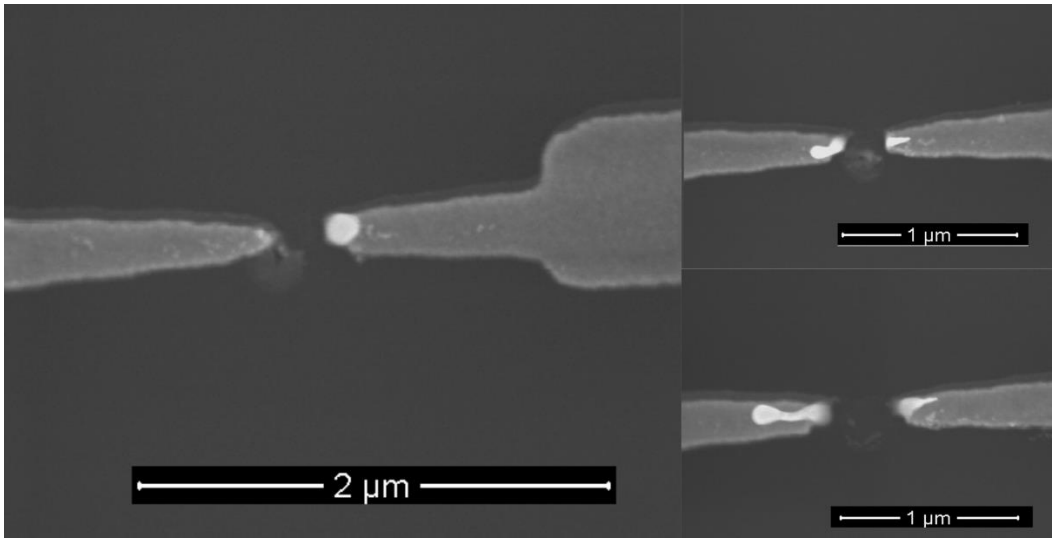

Figure 5.15: Samples damaged during I-V measurements.

5.6 Conclusion

At first, we used E-beam lithography (EBL) to fabricate SETs. The resolution of EBL limits its application to nanostructures with tens of nanometre resolution. Overdosing and shifting techniques were applied to create the tunnelling barrier but no successful fabrication was achieved by this technique. Then, we tried to fabricate the SETs by taking advantage of self - assembled Au nanorods and nano-particles. Although some positive results were obtained, and the desired assembly of NR-NP-NR could be achieved, the lack of facilities hindered further development of this project. Finally, we developed a hybrid fabrication method based on EBL and ALD, and we produced proper SETs. Electrical measurements were performed on our fabricated SETs but the measured I-V did not show the typical curve of a SET. Further investigation revealed that, in all cases, the SETs were damaged during the measurements. This damage was mostly caused by major defects in the electrical measurement setup that caused a sudden change in the electrical potential on the sample and blew it up. Electrical measurements still remain to be performed on our samples.

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