# On the power efficiency, low latency, and quality of service in network-on-chip

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Propositions belonging to the Ph.D. dissertation:

**On the Power Efficiency, Low Latency, and Quality of Service in Network-on-Chip**

by Peng Wang

1. By keeping a certain packet transmission ability in powered-off routers in a Network-on-Chip, the packet latency increase caused by power gating is significantly reduced. (Chapter 3)
2. By bypassing powered-off routers in a Network-on-Chip (NoC), both the power consumption of the NoC and the packet latency increase caused by power gating are significantly reduced. (Chapter 4 and Chapter 5)
3. By clever assignment and scheduling of packets on the resources of a bufferless Network-on-Chip, it is possible to achieve a confined-interference communication in the bufferless NoC. (Chapter 6)
4. By adding a few simple decoders and counters in each router of a bufferless Network-on-Chip (NoC), a confined-interference communication can be realized without a centralized packet scheduler. (Chapter 6)
5. By implementing a Network-on-Chip with more wires but fewer buffers, the design goals of low packet latency, low power consumption, and high bandwidth can be achieved at the same time.
6. The common practice of a single-layer Network-on-Chip (NoC) design must be replaced by a multi-layer NoC design, in order to achieve simpler and more power-efficient NoCs.
7. For implementing a power-efficient large-scale Network-on-Chip (NoC), an asynchronous circuit design has more advantages over a synchronous circuit design.
8. Although a lot of research and development in the field of Network-on-Chip (NoC) design have been done, still the utilization of NoCs in embedded systems is limited.
9. The life of a person is full of ups and downs. The journey of a PhD candidate is full of acceptance and rejection.
10. It is never easy to overcome difficulties, but we can decide whether to enjoy it or suffer from it.