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Fault-tolerant satellite computing with modern semiconductors

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Bibliography

- [1] Directorate of Technical and Quality Management, *ESA/NPI 497-2016: Efficient Dependable Space-Borne Computing through Advanced Reconfigurability Concepts*. ESA, December 2016.
- [2] M. Langer and J. Bouwmeester, “Reliability of CubeSats-statistical data, developers’ beliefs and the way forward,” in *AIAA/USU Conference on Small Satellites (SmallSat)*, 2016.
- [3] M. Swartwout, “The first one hundred CubeSats: A statistical look,” *Journal of Small Satellites*, vol. 2, no. 2, pp. 213–233, 2013.
- [4] E. Stassinopoulos and J. P. Raymond, “The space radiation environment for electronics,” *Proceedings of the IEEE*, vol. 76, no. 11, pp. 1423–1442, 1988.
- [5] J. R. Schwank, M. R. Shaneyfelt, and P. E. Dodd, “Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits,” *IEEE Transactions on Nuclear Science*, 2013.
- [6] L. Whetsel, “An IEEE 1149.1-based test access architecture for ICs with embedded cores,” in *International Test Conference (ITC)*. IEEE, 1997.
- [7] M. R. Patel, *Spacecraft power systems*. CRC press, 2004.
- [8] C. Boshuizen, J. Mason, P. Klupar, and S. Spanhake, “Results from the planet labs flock constellation,” in *AIAA/USU Conference on Small Satellites (SmallSat)*, 2014.
- [9] A. Poghosyan and A. Golkar, “CubeSat evolution: Analyzing CubeSat capabilities for conducting science missions,” *Progress in Aerospace Sciences*, Elsevier, vol. 88, pp. 59–83, 2017.
- [10] T. Wahl, G. K. Høye, A. Lyngvi, and B. T. Narheim, “New possible roles of small satellites in maritime surveillance,” *Acta Astronautica*, Elsevier, vol. 56, no. 1-2, pp. 273–277, 2005.
- [11] M. Parra, A. J. Ricco, B. Yost, M. R. McGinnis, and J. W. Hines, “Studying space effects on microorganisms autonomously: genesat, pharmasat and the future of bio-nanosatellites,” *Gravitational and Space Biology Bulletin*, vol. 21, pp. 9–17, 2008.

- [12] Q. Schiller, D. Gerhardt, L. Blum, X. Li, and S. Palo, “Design and scientific return of a miniaturized particle telescope onboard the colorado student space weather experiment (CSSWE) CubeSat,” in *IEEE Aerospace Conference*. IEEE, 2014.
- [13] C. Underwood, S. Pellegrino, V. J. Lappas, C. P. Bridges, and J. Baker, “Using CubeSat/micro-satellite technology to demonstrate the autonomous assembly of a reconfigurable space telescope (AAReST),” *Acta Astronautica, Elsevier*, vol. 114, pp. 112–122, 2015.
- [14] W. Weiss, S. Rucinski, A. Moffat, A. Schwarzenberg-Czerny, O. Koudelka, C. Grant, R. Zee, R. Kuschnig, J. Matthews, P. Orleanski *et al.*, “Brite-constellation: nanosatellites for precision photometry of bright stars,” *Publications of the Astronomical Society of the Pacific*, vol. 126, no. 940, p. 573, 2014.
- [15] S. Lacour, M. Nowak, P. Bourget, F. Vincent, A. Kellerer, V. Lapeyrère, L. David, A. Le Tiec, O. Straub, and J. Woillez, “Sage: using CubeSats for gravitational wave detection,” in *Space Telescopes and Instrumentation 2018: Ultraviolet to Gamma Ray*, vol. 10699. International Society for Optics and Photonics, 2018, p. 106992R.
- [16] S.-i. Watanabe, Y. Tsuda, M. Yoshikawa, S. Tanaka, T. Saiki, and S. Nakazawa, “Hayabusa2 mission overview,” *Space Science Reviews, Springer*, vol. 208, no. 1-4, pp. 3–16, 2017.
- [17] J. Schoolcraft, A. T. Klesh, and T. Werne, “Marco: interplanetary mission development on a CubeSat scale,” in *Space Operations: Contributions from the Global Community*. Springer, 2017.
- [18] I. F. Akyildiz and A. Kak, “The internet of space things/cubesats: A ubiquitous cyber-physical system for the connected world,” *Computer Networks, Elsevier*, vol. 150, pp. 134–149, 2019.
- [19] M. Cappella, “The principle of equitable access in the age of mega-constellations,” in *Legal Aspects Around Satellite Constellations*. Springer, 2019, pp. 11–23.
- [20] L. Wang, R. Chen, B. Xu, X. Zhang, T. Li, and C. Wu, “The challenges of LEO based navigation augmentation system—lessons learned from Luojia-1a satellite,” in *China Satellite Navigation Conference*. Springer, 2019, pp. 298–310.
- [21] M. Harris, “Tech giants race to build orbital internet [news],” *IEEE Spectrum*, vol. 55, no. 6, pp. 10–11, 2018.
- [22] H. Bedon, C. Negron, J. Llantoy, C. M. Nieto, and C. O. Asma, “Preliminary internetworking simulation of the qb50 CubeSat constellation,” in *IEEE Latin-American Conference on Communications*. IEEE, 2010, pp. 1–6.
- [23] V. L. Foreman, A. Siddiqi, and O. De Weck, “Large satellite constellation orbital debris impacts: case studies of oneweb and spacex proposals,” in *AIAA SPACE and Astronautics Forum and Exposition*, 2017, p. 5200.
- [24] T. Hiriart and J. H. Saleh, “Observations on the evolution of satellite launch volume and cyclicalities in the space industry,” *Space Policy, Elsevier*, vol. 26, no. 1, pp. 53–60, 2010.

- [25] L. D. Feinberg, “Engineering history of the james webb space telescope (JWST) optical telescope element,” 2018, nASA Goddard Space Flight Center.
- [26] F. Lura and D. Hagelschuer, “System conditioning-our ways and testing tools for the development of reliability for spaceborne components and small satellites,” in *Digest of the First International Symposium of the International Academy of Astronautics (IAA), Berlin, November, 1999*, pp. 4–8.
- [27] S. Vinod *et al.*, “Satellite ground testing-objectives and implementation,” *Ground Testing of Aerospace Vehicles Including Engines*, Allied Publishers, p. 223, 1994.
- [28] R. Haefer, “Vacuum and cryotechniques in space research,” *Vacuum*, Elsevier, vol. 22, no. 8, pp. 303–314, 1972.
- [29] D. Koelle, “Specific transportation costs to GEO – past, present and future,” *Acta Astronautica*, Elsevier, vol. 53, no. 4, pp. 797–803, 2003.
- [30] J. N. Pelton, “Launch vehicles and launch sites,” in *Handbook of Satellite Applications*. Springer, 2013, pp. 1131–1144.
- [31] A. L. Weigel and D. E. Hastings, “Evaluating the cost and risk impacts of launch choices,” *Journal of Spacecraft and Rockets*, AIAA, vol. 41, no. 1, pp. 103–110, 2004.
- [32] H. Helvajian and S. Janson, *Small satellites: past, present, and future*. AIAA, 2009.
- [33] J. Depasquale, A. Charania, H. Kanamaya, and S. Matsuda, “Analysis of the earth-to-orbit launch market for nano and microsatellites,” in *AIAA SPACE 2010 Conference & Exposition*, 2010, p. 8602.
- [34] D. DePasquale and J. Bradford, “Nano/microsatellite market assessment,” *Public Release, Revision A, SpaceWorks*, 2013.
- [35] B. Twiggs, S. Lee, A. Hutputanasin, A. Toorian, W. Lan, R. Munakata, J. Carnahan, D. Pignatelli, A. Mehrparvar *et al.*, “CubeSat design specification rev. 13,” Cal Poly SLO, Standard, 2015.
- [36] M. Czech, A. Fleischner, and U. Walter, “A first-move in satellite development at the tu-münchen,” in *Small Satellite Missions for Earth Observation*. Springer, 2010, pp. 235–245.
- [37] D. J. Barnhart, T. Vladimirova, A. M. Baker, and M. N. Sweeting, “A low-cost femtosatellite to enable distributed space missions,” *Acta Astronautica*, Elsevier, vol. 64, no. 11-12, pp. 1123–1143, 2009.
- [38] J. Tristanco and J. Gutierrez-Cabello, “A probe of concept for femto-satellites based on commercial-of-the-shelf,” in *IEEE/AIAA Digital Avionics Systems Conference*. IEEE, 2011, pp. 8A2–1.
- [39] J. Bouwmeester, M. Langer, and E. Gill, “Survey on the implementation and reliability of CubeSat electrical bus interfaces,” *CEAS Space Journal*, Springer, vol. 9, no. 2, pp. 163–173, 2017.

- [40] R. Carlson, K. Hand, and E. Ozer, “On the use of System-on-Chip technology in next-generation instruments avionics for space exploration,” in *IFIP/IEEE International Conference on Very Large Scale Integration-System on a Chip (VLSI-SoC), revised paper*. Springer, 2016.
- [41] M. Swartwout, “The first one hundred CubeSats: A statistical look,” *Journal of Small Satellites*, 2014.
- [42] M. Swartwout, “You say ‘PicoSat’, i say ‘CubeSat’: Developing a better taxonomy for secondary spacecraft,” in *IEEE Aerospace Conference*, 2018.
- [43] M. Swartwout, “Cubesats and mission success: A look at the numbers,” in *CubeSat Developers Workshop*. CalPoly, 2016.
- [44] R. Trivedi and U. S. Mehta, “A survey of radiation hardening by design (RHBD) techniques for electronic systems for space application,” *International Journal of Electronics and Communication Engineering & Technology (IJECET)*, vol. 7, no. 1, p. 75, 2016.
- [45] P. Roche, J.-L. Autran, G. Gasiot, and D. Munteanu, “Technology downscaling worsening radiation effects in bulk: SOI to the rescue,” in *IEEE International Electron Devices Meeting*. IEEE, 2013, pp. 31–1.
- [46] S. M. Guertin, M. Amrbar, and S. Vartanian, “Radiation test results for common CubeSat microcontrollers and microprocessors,” in *IEEE Radiation Effects Data Workshop (REDW)*. IEEE, 2015, pp. 1–9.
- [47] D. Selčan, G. Kirbiš, and I. Kramberger, “Low level radiation and fault protection techniques suitable for nanosatellite missions,” in *Conference on Radiation and its Effects on Components and Systems (RADECS)*. IEEE, 2017.
- [48] M. Swartwout, “Secondary spacecraft in 2016: Why some succeed (and too many do not),” in *IEEE Aerospace Conference*. IEEE, 2016, pp. 1–13.
- [49] M. Williamson, “Commercial space risks, spacecraft insurance, and the fragile frontier,” in *Frontiers of Space Risk*. CRC Press, 2018, pp. 143–163.
- [50] J. R. Samson, “Update on dependable multiprocessor CubeSat technology development,” in *2012 IEEE Aerospace Conference*. IEEE, 2012, pp. 1–12.
- [51] B. S. Dhillon, *Human reliability: with human factors*. Elsevier, 2013.
- [52] R. Isermann, *Fault-diagnosis systems: an introduction from fault detection to fault tolerance*. Springer Science & Business Media, 2006.
- [53] I. P. Egwuatuoha, D. Levy, B. Selic, and S. Chen, “A survey of fault tolerance mechanisms and checkpoint/restart implementations for high performance computing systems,” *Journal of Supercomputing*, vol. 65, no. 3, pp. 1302–1326, 2013.
- [54] R. Ginosar, “Survey of processors for space,” *Eurospace Data Systems In Aerospace (DASIA)*, 2012.
- [55] K. Tindell, H. Hanssmon, and A. J. Wellings, “Analysing real-time communications: Controller area network (CAN).” in *Real Time System Symposium (RTSS)*. IEEE, 1994, pp. 259–263.

- [56] R. Makowitz and C. Temple, "Flexray—a communication network for automotive control systems," in *IEEE International Workshop on Factory Communication Systems*. IEEE, 2006, pp. 207–212.
- [57] W. R. Moore, "A review of fault-tolerant techniques for the enhancement of integrated circuit yield," *Proceedings of the IEEE*, vol. 74, no. 5, pp. 684–698, 1986.
- [58] L. Jiang, R. Ye, and Q. Xu, "Yield enhancement for 3d-stacked memory by redundancy sharing across dies," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*. IEEE, 2010, pp. 230–234.
- [59] P. A. Buckland, J. R. Herring, G. M. Nordstrom, and W. A. Thompson, "Cable redundancy and failover for multi-lane pci express io interconnections," Mar. 18 2014, US Patent 8,677,176.
- [60] B. Vucetic and J. Yuan, *Turbo codes: principles and applications*. Springer Science & Business Media, 2012, vol. 559.
- [61] Z. Zhang, V. Anantharam, M. J. Wainwright, and B. Nikolic, "An efficient 10gbase-t ethernet ldpc decoder design with low error floors," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 843–855, 2010.
- [62] Y. Furukawa, "Intellectual property protection and innovation: An inverted-u relationship," *Economics Letters*, Elsevier, vol. 109, no. 2, pp. 99–101, 2010.
- [63] M. Fidler and A. Rizk, "A guide to the stochastic network calculus," *IEEE Communications Surveys & Tutorials*, vol. 17, no. 1, pp. 92–105, 2014.
- [64] K. Suresh, C. W. Selvidge, S. Gupta, and A. Jain, "Debug environment for a multi user hardware assisted verification system," Feb. 1 2018, US Patent App. 15/646,003.
- [65] M. Kooli and G. Di Natale, "A survey on simulation-based fault injection tools for complex systems," in *International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*. IEEE, 2014.
- [66] H. Ziade, R. A. Ayoubi, R. Velazco *et al.*, "A survey on fault injection techniques," *Int. Arab J. Inf. Technol.*, vol. 1, no. 2, pp. 171–186, 2004.
- [67] M. M. Hassan, W. Afzal, M. Blom, B. Lindström, S. F. Andler, and S. Eldh, "Testability and software robustness: A systematic literature review," in *Euromicro Conference on Software Engineering and Advanced Applications*. IEEE, 2015.
- [68] J. W. Bennett, G. J. Atkinson, B. C. Mecrow, and D. J. Atkinson, "Fault-tolerant design considerations and control strategies for aerospace drives," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 5, pp. 2049–2058, 2011.
- [69] G. C. Clark Jr and J. B. Cain, *Error-correction coding for digital communications*. Springer Science & Business Media, 2013.
- [70] P. W. Coteus, H. C. Hunter, C. A. Kilmer, K.-h. Kim, L. A. Lastras-Montano, W. E. Maule, and V. Patel, "Error feedback and logging with memory on-chip error checking and correcting (ECC)," Jan. 30 2018, US Patent 9,880,896.

- [71] M. Tipaldi and B. Bruenjes, “Survey on fault detection, isolation, and recovery strategies in the space domain,” *Journal of Aerospace Information Systems*, vol. 12, no. 2, pp. 235–256, 2015.
- [72] D. A. Patterson, G. Gibson, and R. H. Katz, *A case for redundant arrays of inexpensive disks (RAID)*. ACM, 1988, vol. 17, no. 3.
- [73] P. R. Grams, “Ethernet for aerospace applications-ethernet heads for the skies,” in *IEEE Ethernet Technology Summit*. NASA, 2015.
- [74] M. Luby, L. Vicisano, J. Gemmell, L. Rizzo, M. Handley, and J. Crowcroft, “RFC 5052: Forward error correction (FEC) building block,” IETF, Tech. Rep., 2007.
- [75] D. Boley, G. H. Golub, S. Makar, N. Saxena, and E. J. McCluskey, “Floating point fault tolerance with backward error assertions,” *IEEE Transactions on Computers*, vol. 44, no. 2, pp. 302–311, 1995.
- [76] R. C. Aitken, “Modeling the unmodelable: Algorithmic fault diagnosis,” *IEEE Design & Test of Computers*, vol. 14, no. 3, pp. 98–103, 1997.
- [77] J. Sloan, R. Kumar, and G. Bronevetsky, “Algorithmic approaches to low overhead fault detection for sparse linear algebra,” in *Conference on Dependable Systems and Networks (DSN)*. IEEE, 2012.
- [78] N. R. Saxena and E. J. McCluskey, “Control-flow checking using watchdog assists and extended-precision checksums,” *IEEE Transactions on Computers*, vol. 39, no. 4, pp. 554–559, 1990.
- [79] S. Z. Shazli and M. B. Tahoori, “Transient error detection and recovery in processor pipelines,” in *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*. IEEE, 2009, pp. 304–312.
- [80] J. Gaisler, “Concurrent error-detection and modular fault-tolerance in a 32-bit processing core for embedded space flight applications,” in *IEEE International Symposium on Fault-Tolerant Computing (FTCS)*. IEEE, 1994, pp. 128–130.
- [81] S. Agrawal and K. Daudjee, “A performance comparison of algorithms for byzantine agreement in distributed systems,” in *European Dependable Computing Conference (EDCC)*. IEEE, 2016.
- [82] M. Barborak, A. Dahbura, and M. Malek, “The consensus problem in fault-tolerant computing,” *ACM Computing Surveys (CSur)*, vol. 25, no. 2, pp. 171–220, 1993.
- [83] T. Jackson, B. Salamat, A. Homescu, K. Manivannan, G. Wagner, A. Gal, S. Brunthaler, C. Wimmer, and M. Franz, “Compiler-generated software diversity,” in *Moving Target Defense*. Springer, 2011, pp. 77–98.
- [84] S. Punnekkat, A. Burns, and R. Davis, “Analysis of checkpointing for real-time systems,” *Real-Time Systems, Springer*, vol. 20, no. 1, pp. 83–102, 2001.
- [85] A. Thekkilakattil, R. Dobrin, and S. Punnekkat, “Fault tolerant scheduling of mixed criticality real-time tasks under error bursts,” *Procedia Computer Science, Elsevier*, vol. 46, pp. 1148–1155, 2015.

- [86] ——, “Bounding the effectiveness of temporal redundancy in fault-tolerant real-time scheduling under error bursts,” in *IEEE Emerging Technology and Factory Automation (ETFA)*. IEEE, 2014, pp. 1–8.
- [87] M. Short and J. Proenza, “Towards efficient probabilistic scheduling guarantees for real-time systems subject to random errors and random bursts of errors,” in *Euromicro Conference on Real-Time Systems*. IEEE, 2013, pp. 259–268.
- [88] X. Iturbe, B. Venu, E. Ozer, and S. Das, “A triple core lock-step (TCLS) ARM Cortex-R5 processor for safety-critical and ultra-reliable applications,” in *Conference on Dependable Systems and Networks Workshop (DSN-W)*. IEEE, 2016.
- [89] J. Arm, Z. Bradac, and R. Stohl, “Increasing safety and reliability of roll-back and roll-forward lockstep technique for use in real-time systems,” *IFAC Conference on Programmable Devices and Embedded Systems (PDES)*, Elsevier, vol. 49, no. 25, pp. 413–418, 2016.
- [90] K. D. Safford, D. C. Soltis Jr, and E. R. Delano, “Off-chip lockstep checking,” Jun. 26 2007, US Patent 7,237,144.
- [91] B. H. Meyer, B. H. Calhoun, J. Lach, and K. Skadron, “Cost-effective safety and fault localization using distributed temporal redundancy,” in *International Conference on Compilers, architectures and synthesis for embedded systems*. ACM, 2011, pp. 125–134.
- [92] Y. Zhou, X. Wang, Y. Chen, and Z. Wang, “Armlock: Hardware-based fault isolation for arm,” in *ACM SIGSAC conference on computer and communications security*. ACM, 2014, pp. 558–569.
- [93] J. Zhou, H. Li, T. Wang, and X. Li, “Loft: A low-overhead fault-tolerant routing scheme for 3D NoCs,” *Integration, the VLSI Journal*, 2016.
- [94] Aeronautical Radio, INC, *ARINC Specification 664: Avionics Full Duplex Switched Ethernet (AFDX)*, 2005.
- [95] Y. Li, E. L. Miller, and D. D. Long, “Understanding data survivability in archival storage systems,” in *International Systems and Storage Conference*. ACM, 2012.
- [96] N. Joukov, A. M. Krishnakumar, C. Patti, A. Rai, S. Satnur, A. Traeger, and E. Zadok, “RAIF: Redundant array of independent filesystems,” in *Conference on Mass Storage Systems and Technologies (MSST)*. IEEE, 2007, pp. 199–214.
- [97] M.-A. Song, S.-Y. Kuo, and I.-F. Lan, “A low complexity design of Reed-Solomon code algorithm for advanced RAID system,” *IEEE Transactions on Consumer Electronics (TCE)*, vol. 53, 2007.
- [98] R. L. Alena, J. P. Ossenfort, K. I. Laws, A. Goforth, and F. Figueira, “Communications for integrated modular avionics,” in *IEEE Aerospace Conference*. IEEE, 2007, pp. 1–18.
- [99] M. Roa, W. Cantrell, D. Cartes, and M. Nelson, “Requirements for deterministic control systems,” in *IEEE Electric Ship Technologies Symposium*. IEEE, 2011, pp. 439–445.

- [100] S. V. Amari and G. Dill, "Redundancy optimization problem with warm-standby redundancy," in *Reliability and Maintainability Symposium (RAMS)*. IEEE, 2010.
- [101] ——, "A new method for reliability analysis of standby systems," in *Reliability and Maintainability Symposium (RAMS)*. IEEE, 2009.
- [102] J. J. Wylie and R. Swaminathan, "Selecting erasure codes for a fault tolerant system," Aug. 21 2012, US Patent 8,250,427.
- [103] J. S. Plank, "A tutorial on reed-solomon coding for fault-tolerance in raid-like systems," *Software: Practice and Experience*, vol. 27, no. 9, pp. 995–1012, 1997.
- [104] M. Hijorth, M. Aberg, N.-J. Wessman, J. Andersson, R. Chevallier, R. Forsyth, R. Weigand, and L. Fossati, "GR740: Rad-hard quad-core LEON4FT system-on-chip," in *Eurospace Data Systems In Aerospace (DASIA)*, 2015.
- [105] L. Bozzoli and L. Sterpone, "Self rerouting of dynamically reconfigurable SRAM-based FPGAs," in *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*. IEEE, 2017.
- [106] R. Baheti and H. Gill, "Cyber-physical systems," *The impact of control technology, IEEE Control Systems Society*, vol. 12, no. 1, pp. 161–166, 2011.
- [107] M. D. Berg, H. S. Kim, A. M. Phan, C. M. Seidleck, K. A. LaBel, J. A. Pellish, and M. J. Campola, "The effects of race conditions when implementing single-source redundant clock trees in triple modular redundant synchronous architectures," in *Conference on Radiation and its Effects on Components and Systems (RADECS)*. IEEE, 2016.
- [108] M. Berg, K. LaBel, M. Campola, and M. Xapsos, "Analyzing system on a chip single event upset responses using single event upset data, classical reliability models, and space environment data," in *Conference on Radiation and its Effects on Components and Systems (RADECS)*. IEEE, 2017.
- [109] G. G. Preckshot, *Method for performing diversity and defense-in-depth analyses of reactor protection systems*. Division of Reactor Controls and Human Factors, Office of Nuclear Reactor Regulation, US Nuclear Regulatory Commission, 1994.
- [110] D. K. Nilsson and U. Larson, "A defense-in-depth approach to securing the wireless vehicle infrastructure," *Journal of Networks (JNW)*, vol. 4, no. 7, pp. 552–564, 2009.
- [111] T. G. Rauscher, "Raid system with multiple controllers and proof against any single point of failure," Mar. 29 2005, US Patent 6,874,100.
- [112] H. Madeira, R. R. Some, F. Moreira, D. Costa, and D. Rennels, "Experimental evaluation of a cots system for space applications," in *Proceedings International Conference on Dependable Systems and Networks*. IEEE, 2002, pp. 325–330.
- [113] J. Hammarberg and S. Nadjm-Tehrani, "Formal verification of fault tolerance in safety-critical reconfigurable modules," *Journal on Software Tools for Technology Transfer, Springer*, vol. 7, no. 3, pp. 268–279, 2005.

- [114] X. Cai and M. R. Lyu, "Software reliability modeling with test coverage: Experimentation and measurement with a fault-tolerant software project," in *IEEE International Symposium on Software Reliability (ISSRE)*. IEEE, 2007, pp. 17–26.
- [115] J. L. Nunes, T. Pecserke, J. C. Cunha, and M. Zenha-Rela, "FIRED—fault injector for reconfigurable embedded devices," in *IEEE Pacific Rim International Symposium on Dependable Computing (PRDC)*. IEEE, 2015.
- [116] I. Sommerville, "Software engineering (10th edition)," *ISBN-10*, vol. 0133943038, 2015.
- [117] B. Schroeder, E. Pinheiro, and W.-D. Weber, "DRAM errors in the wild: a large-scale field study," *Communications of the ACM*, vol. 54, no. 2, pp. 100–107, 2011.
- [118] A. Mukati, "A survey of memory error correcting techniques for improved reliability," *Journal of Network and Computer Applications*, Elsevier, vol. 34, no. 2, pp. 517–522, 2011.
- [119] T. Lanier, "Exploring the design of the cortex-a15 processor," https://www.arm.com/files/pdf/AT-Exploring_the_Design_of_the_Cortex-A15.pdf, 2011.
- [120] USB-IF, "Universal serial bus revision 3.1 specification," 2011.
- [121] K. Deyring *et al.*, "Serial ATA: High speed serialized at attachment," *Jan*, vol. 7, pp. 1–22, 2003.
- [122] P. Savio, A. Nespola, S. Straullu, S. Abrate, and R. Gaudino, "A physical coding sublayer for gigabit ethernet over POF," in *International Conference on Plastic Optical Fibers (POF)*. International Cooperative of Plastic Optical Fibers, 2010.
- [123] A. Goldhammer and J. Ayer Jr, "Understanding performance of pci express systems," *Xilinx WP350, Sept*, vol. 4, 2008.
- [124] H. Zhang, S. Krooswyk, and J. Ou, *High Speed Digital Design: Design of High Speed Interconnects and Signaling*. Elsevier, 2015.
- [125] R. Micheloni, A. Marelli, and K. Eshghi, *Inside solid state drives (SSDs)*. Springer, 2013.
- [126] C. W. Slayman, "Cache and memory error detection, correction, and reduction techniques for terrestrial servers and workstations," *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 3, pp. 397–404, 2005.
- [127] L. L. Pullum, *Software fault tolerance techniques and implementation*. Artech House, 2001.
- [128] N. Diniz and J. Rufino, "ARINC 653 in space," in *Eurospace Data Systems In Aerospace (DASIA)*, 2005.
- [129] J. Teich, "Hardware/software codesign: The past, the present, and predicting the future," *Proceedings of the IEEE*, vol. 100, no. Special Centennial Issue, pp. 1411–1430, 2012.

- [130] W. Bartlett and L. Spainhower, “Commercial fault tolerance: A tale of two systems,” *IEEE Transactions on dependable and secure computing*, vol. 1, no. 1, pp. 87–96, 2004.
- [131] T. Slivinski, C. Broglio, C. Wild, J. Goldberg, K. Levitt, E. Hitt, and J. Webb, “Study of fault-tolerant software technology,” NASA, Technical Report, 1984.
- [132] K. Reick, P. N. Sanda, S. Swaney, J. W. Kellington, M. Mack, M. Floyd, and D. Henderson, “Fault-tolerant design of the ibm power6 microprocessor,” *IEEE micro*, vol. 28, no. 2, pp. 30–38, 2008.
- [133] C. C. Reed, R. Bri  t, M. Begert, and T. Newbauer, “Esd detection, location and mitigation, and why they are important for satellite development,” in *Spacecraft Charging Technology Conference*, 2014.
- [134] S. Bourdarie and M. Xapsos, “The Near-Earth Space Radiation Environment,” *IEEE Transactions on Nuclear Science*, 2008.
- [135] Xapsos, O’Neill, and T. P. O’Brien, “Near-Earth Space Radiation Models,” *IEEE Transactions on Nuclear Science*, 2013.
- [136] J. Heirtzler, “The future of the south atlantic anomaly and implications for radiation damage in space,” *Journal of Atmospheric and Solar-Terrestrial Physics*, Elsevier, 2002.
- [137] ECSS, “Calculation of radiation and its effects and margin policy handbook,” 2010.
- [138] T. Amort, “Radiation-hardening by design phase 3,” in *Microelectronics Reliability and Qualification Workshop (MRQW)*. The Aerospace Corporation, 2013.
- [139] P. Mishra, A. Muttreja, and N. K. Jha, “FinFET circuit design,” in *Nanoelectronic Circuit Design*. Springer, 2011, pp. 23–54.
- [140] S. A. Vitale, P. W. Wyatt, N. Checka, J. Kedzierski, and C. L. Keast, “FDSOI process technology for subthreshold-operation ultralow-power electronics,” *Proceedings of the IEEE*, vol. 98, no. 2, pp. 333–342, 2010.
- [141] M. Alles, R. Schrimpf, R. Reed, L. Massengill, R. Weller, M. Mendenhall, D. Ball, K. Warren, T. Loveless, J. Kauppila *et al.*, “Radiation hardness of FDSOI and FinFET technologies,” in *IEEE International SOI Conference*. IEEE, 2011.
- [142] L. A. Tambara, F. L. Kastensmidt, N. H. Medina, N. Added, V. A. Aguiar, F. Aguirre, E. L. Macchione, and M. A. Silveira, “Heavy ions induced single event upsets testing of the 28 nm Xilinx Zynq-7000 all programmable SoC,” in *IEEE Radiation Effects Data Workshop (REDW)*, 2015.
- [143] M. D. Berg, K. A. LaBel, and J. Pellish, “Single event effects in FPGA devices 2014-2015,” in *NASA NEPP Electronics Technology Workshop*, 2015.
- [144] M. Kochiyama, T. Sega, K. Hara, Y. Arai, T. Miyoshi, Y. Ikegami, S. Terada, Y. Unno, K. Fukuda, and M. Okihara, “Radiation effects in Silicon-on-Insulator transistors with back-gate control method fabricated with OKI semiconductor 0.20 μm FD-SOI technology,” *Nuclear Instruments and Methods in Physics Research*, Elsevier, 2011.

- [145] H. Hayat, K. Kohary, and C. D. Wright, “Can conventional phase-change memory devices be scaled down to single-nanometre dimensions?” *Nanotechnology, IOP Publishing*, 2016.
- [146] A. Fert, J.-M. George, H. Jaffrè, R. Mattana, and P. Seneor, “The new era of spintronics,” *Europhysics news, EDP Sciences*, vol. 34, no. 6, pp. 227–229, 2003.
- [147] J.-C. Wu, H. L. Stadler, and R. R. Katti, “High speed magneto-resistive random access memory,” Dec. 22 1992, US Patent 5,173,873.
- [148] D. Chen, H. Kim, A. Phan, E. Wilcox, K. LaBel, S. Buchner, A. Khachatrian, and N. Roche, “Single-event effect performance of a commercial embedded reram,” *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3088–3094, 2014.
- [149] F. Chen, “Phase-change memory,” Feb. 26 2014, US Patent App. 14/191,016.
- [150] G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, A. Todri, A. Virazel, S. McClure, A. Touboul, F. Wrobel, and F. Saigné, “Testing a Commercial MRAM Under Neutron and Alpha Radiation in Dynamic Mode,” *IEEE Transactions on Nuclear Science*, 2013.
- [151] J. Maimon, K. Hunt, J. Rodgers, L. Burcin, and K. Knowles, “Results of radiation effects on a chalcogenide non-volatile memory array,” in *IEEE Aerospace Conference*, 2004.
- [152] J. P. van Zandwijk and A. Fukami, “NAND flash memory forensic analysis and the growing challenge of bit errors,” *IEEE Security & Privacy*, vol. 15, no. 6, pp. 82–87, 2017.
- [153] S. Gerardin, M. Bagatin, A. Paccagnella, K. Grümann, F. Gliem, T. Oldham, F. Irom, and D. N. Nguyen, “Radiation Effects in Flash Memories,” *IEEE Transactions on Nuclear Science*, 2013.
- [154] C. Poivey, “Total ionizing dose (TID) and total non ionizing dose (TNID) effects in electronic parts,” Lecture Notes of the School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA), 2018.
- [155] T. Oldham, M. Suhail, M. Friendlich, M. Carts, R. Ladbury, H. Kim, M. Berg, C. Poivey, S. Buchner, A. Sanders *et al.*, “TID and SEE response of advanced 4g NAND flash memories,” in *IEEE Radiation Effects Data Workshop (REDW)*. IEEE, 2008, pp. 31–37.
- [156] K. Young *et al.*, “SLC vs. MLC: An analysis of flash memory,” *Whitepaper, Super Talent Technology, Inc.*, 3 2008.
- [157] S. Gerardin and A. Paccagnella, “Present and future non-volatile memories for space,” *IEEE Transactions on Nuclear Science*, vol. 57, 2010.
- [158] K. Gupta and K. Kirby, “Mitigation of high altitude and low earth orbit radiation effects on microelectronics via shielding or error detection and correction systems,” NASA, Tech. Rep., 2004.

- [159] B. Klamm, “Passive space radiation shielding: Mass and volume optimization of tungsten-doped polyphenolic and polyethylene resins,” in *AIAA/USU Conference on Small Satellites (SmallSat)*, 2015.
- [160] E. Benton and E. Benton, “A survey of radiation measurements made aboard russian spacecraft in low-earth orbit,” NASA, Tech. Rep., 1999.
- [161] M. Poizat, M. Sauvagnac, A. Samaras, Y. Padie, P. Garcia, B. Renaud, L. Gouyet, J. P. Abadi, F. Widmeer, E. Le Goulven *et al.*, “Compendium of total ionizing dose, displacement damage and single event transient test data of various optocouplers for esa,” in *IEEE Radiation Effects Data Workshop (REDW)*. IEEE, 2013, pp. 1–6.
- [162] A. E. Bergles, “Evolution of cooling technology for electrical, electronic, and microelectronic equipment,” *IEEE Transactions on Components and Packaging Technologies*, 2003.
- [163] K. Puttaswamy and G. H. Loh, “Thermal herding: Microarchitecture techniques for controlling hotspots in high-performance 3d-integrated processors,” in *International Symposium on High Performance Computer Architecture (HPCA)*. IEEE, 2007.
- [164] D. G. Gilmore and M. Donabedian, *Spacecraft thermal control handbook: cryogenics*. AIAA, 2003, vol. 2.
- [165] B. Wood, W. Bertrand, R. Bryson, B. Seiber, and P. M. FALCO, “Surface effects of satellite material outgassing products,” *Journal of Thermophysics and Heat Transfer, AIAA*, vol. 2, no. 4, pp. 289–295, 1988.
- [166] B. R. Spence, S. White, M. LaPointe, S. Kiefer, P. LaCorte, J. Banik, D. Chapman, and J. Merrill, “International space station (ISS) roll-out solar array (ROSA) spaceflight experiment mission and results,” in *IEEE World Conference on Photovoltaic Energy Conversion (WCPEC)*. IEEE, 2018, pp. 3522–3529.
- [167] R. Gubby and J. Evans, “Space environment effects and satellite design,” *Journal of Atmospheric and Solar-Terrestrial Physics, Elsevier*, vol. 64, no. 16, pp. 1723–1733, 2002.
- [168] A. Driskill-Smith, D. Apalkov, V. Nikitin, X. Tang, S. Watts, D. Lottis, K. Moon, A. Khvalkovskiy, R. Kawakami, X. Luo *et al.*, “Latest advances and roadmap for in-plane and perpendicular STT-RAM,” in *IEEE International Memory Workshop (IMW)*. IEEE, 2011, pp. 1–3.
- [169] V. Dos Santos Paulino, “Influence of risk on technology adoption: inertia strategy in the space industry,” *European Journal of Innovation Management*, vol. 17, no. 1, pp. 41–60, 2014.
- [170] C. Boshuizen, W. Marshall, C. Bridges, S. Kenyon, and P. Klupar, “Learning to follow: Embracing commercial technologies and open source for space missions,” in *International Astronautical Congress (IAC’11)*, no. IAC-11, 2011.
- [171] G. Dubos, J. Saleh, and R. Braun, “Technology readiness level, schedule risk and slippage in spacecraft design: Data analysis and modeling,” in *AIAA SPACE 2007 conference & exposition*, 2007, p. 6020.

- [172] D. M. Waltz, *On-orbit servicing of space systems*. Krieger Pub Co, 1993.
- [173] D. E. Hastings and C. Joppin, “On-orbit upgrade and repair: The hubble space telescope example,” *Journal of spacecraft and rockets, AIAA*, vol. 43, no. 3, pp. 614–625, 2006.
- [174] A. Long, M. Richards, and D. E. Hastings, “On-orbit servicing: a new value proposition for satellite design and operation,” *Journal of Spacecraft and Rockets*, vol. 44, no. 4, pp. 964–976, 2007.
- [175] L. Crane, “Crunch time in orbit,” 2018, elsevier.
- [176] J. L. Webster, “Cassini spacecraft engineering tutorial,” 2006, nASA/Jet Propulsion Lab.
- [177] R. D. Lange, “Cassini-huygens mission overview and recent science results,” in *IEEE Aerospace Conference*. IEEE, 2008, pp. 1–10.
- [178] G. Maral and M. Bousquet, *Satellite communications systems: systems, techniques and technology*. John Wiley & Sons, 2011.
- [179] W. Larson, J. Wertz, and B. D’Souza, *SMAD III: Space Mission Analysis and Design, 3rd Edition: Workbook*, ser. Space technology library. Microcosm Press, 2005.
- [180] S. Cakaj, W. Keim, and K. Malarić, “Communications duration with low earth orbiting satellites,” in *IASTED International Conference on Antennas, Radar and Wave Propagation (ARP)*. ACTA Press, 2007.
- [181] S. H. Schaire, S. Altunc, G. Bussey, H. Shaw, B. Horne, and J. Schier, “NASA near earth network (NEN), deep space network (DSN) and space network (SN) support of CubeSat communications,” in *NASA SpaceOps Workshop*. NASA, 2015.
- [182] Y. Nakamura, S. Nakasuka, and Y. Oda, “Low-cost and reliable ground station network to improve operation efficiency for micro/nano-satellites,” in *International Astronautical Congress (IAC)*, 2005.
- [183] R. Welch, D. Limonadi, and R. Manning, “Systems engineering the curiosity rover: A retrospective,” in *International Conference on System of Systems Engineering*. IEEE, 2013, pp. 70–75.
- [184] R. Ludwig and J. Taylor, *Voyager telecommunications*. John Wiley and Sons, Inc, 2016.
- [185] J. Taylor, *Deep Space Communications*. John Wiley & Sons, 2016.
- [186] K. Reh, L. Spilker, J. I. Lunine, J. H. Waite, M. L. Cable, F. Postberg, and K. Clark, “Enceladus life finder: the search for life in a habitable moon,” in *IEEE Aerospace Conference*. IEEE, 2016, pp. 1–8.
- [187] B. Bastida Virgili and H. Krag, “Mega-constellations issues,” in *COSPAR Scientific Assembly*, 2016.

- [188] A. S. Jackson, “Implementation of the configurable fault tolerant system experiment on NPSAT-1,” Ph.D. dissertation, Naval Postgraduate School Monterey, 2016.
- [189] D. Lüdtke, K. Westerdorff, K. Stohlmann, A. Börner, O. Maibaum, T. Peng, B. Weps, G. Fey, and A. Gerndt, “OBC-NG: towards a reconfigurable on-board computing architecture for spacecraft,” in *IEEE Aerospace*, 2014.
- [190] S. Gupta, N. Gala, G. Madhusudan, and V. Kamakoti, “SHAKTI-F: A fault tolerant microprocessor architecture,” in *IEEE Asian Test Symposium (ATS)*, 2015.
- [191] R. DeCoursey, R. Melton, and R. R. Estes, “Non-radiation hardened microprocessors in space-based remote sensing systems,” in *Sensors, Systems, and Next-Generation Satellites X*, vol. 6361. International Society for Optics and Photonics, 2006, p. 63611M.
- [192] M. Pigno *et al.*, “A testbench for validation of DST fault-tolerant architectures on PowerPC G4 COTS microprocessors,” in *Eurospace Data Systems In Aerospace (DASIA)*, 2011.
- [193] M. Pignol, “DMT and DT2,” in *IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS)*, 2006.
- [194] C. A. Hulme, H. H. Loomis, A. A. Ross, and R. Yuan, “Configurable fault-tolerant processor (CFTP) for spacecraft onboard processing,” in *IEEE Aerospace Conference*, 2004.
- [195] J. R. Samson, “Implementation of a dependable multiprocessor CubeSat,” in *IEEE Aerospace*, 2011.
- [196] X. Iturbe, D. Keymeulen, P. Yiu, D. Berisford, R. Carlson, K. Hand, and E. Ozer, “On the use of system-on-chip technology in next-generation instruments avionics for space exploration,” in *IFIP/IEEE International Conference on Very Large Scale Integration-System on a Chip (VLSI-SoC)*. Springer, 2015, pp. 1–22.
- [197] M. Marinella and H. Barnaby, “Total ionizing dose and displacement damage effects in embedded memory technologies,” Sandia National Laboratories, Tech. Rep., 2013.
- [198] U. Kretzschmar, J. Gomez-Cornejo, A. Astarloa, U. Bidarte, and J. Del Ser, “Synchronization of faulty processors in coarse-grained TMR protected partially reconfigurable FPGA designs,” *Reliability Engineering & System Safety*, Elsevier, vol. 151, pp. 1–9, 2016.
- [199] B. Döbel, “Operating system support for redundant multithreading,” Ph.D. dissertation, Dresden University, 2014.
- [200] A. Shye, T. Moseley, V. J. Reddi, J. Blomstedt, and D. A. Connors, “Using process-level redundancy to exploit multiple cores for transient fault tolerance,” in *Conference on Dependable Systems and Networks (DSN)*. IEEE, 2007.
- [201] Y. Dong, W. Ye, Y. Jiang, I. Pratt, S. Ma, J. Li, and H. Guan, “COLO: COarse-grained LOck-stepping virtual machines for non-stop service,” in *Symposium on Cloud Computing (SoCC)*. ACM, 2013.

- [202] A. L. Sartor, A. F. Lorenzon, L. Carro, F. Kastensmidt, S. Wong, and A. Beck, “Exploiting idle hardware to provide low overhead fault tolerance for VLIW processors,” *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, 2017.
- [203] F. Anjam and S. Wong, “Configurable fault-tolerance for a configurable VLIW processor,” in *International Symposium on Applied Reconfigurable Computing (ARC)*, Springer, 2013.
- [204] J. Hursey, J. M. Squyres, T. I. Mattox, and A. Lumsdaine, “The design and implementation of checkpoint/restart process fault tolerance for Open MPI,” in *IEEE International Parallel and Distributed Processing Symposium*. IEEE, 2007, pp. 1–8.
- [205] P. Munk, M. S. Alhakeem, R. Lisicki, H. Parzy jegla, J. Richling, and H.-U. Heiss, “Toward a fault-tolerance framework for COTS many-core systems,” in *European Dependable Computing Conference (EDCC)*. IEEE, 2015.
- [206] L. Zeng, P. Huang, and L. Thiele, “Towards the design of fault-tolerant mixed-criticality systems on multicores,” in *International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, ACM, 2016.
- [207] S. P. Azad, B. Niazmand, J. Raik, G. Jervan, and T. Hollstein, “Holistic approach for fault-tolerant network-on-chip based many-core systems,” *HiPEAC DREAM-Cloud*, ACM, 2016.
- [208] A. Höller, T. Rauter, J. Iber, G. Macher, and C. Kreiner, “Software-based fault recovery via adaptive diversity for COTS multi-core processors,” 2015, arXiv:1511.03528.
- [209] A. D. Santangelo, “An open source space hypervisor for small satellites,” in *AIAA SPACE*, 2013.
- [210] E. Missimer, R. West, and Y. Li, “Distributed real-time fault tolerance on a virtualized multi-core system,” *Euromicro Conference on Real-Time Systems (ECRTS/OSPERT)*, 2014.
- [211] Z. Al-bayati, B. H. Meyer, and H. Zeng, “Fault-tolerant scheduling of multi-core mixed-criticality systems under permanent failures,” in *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, 2016.
- [212] S. Malik and F. Huet, “Adaptive fault tolerance in real time cloud computing,” in *IEEE World Congress on Services (SERVICES)*, 2011.
- [213] K. Smiri, S. Bekri, and H. Smei, “Fault-tolerant in embedded systems (MPSoC): Performance estimation and dynamic migration tasks,” in *IEEE International Design & Test Symposium (IDT)*, 2016.
- [214] Z. Al-bayati, J. Caplan, B. H. Meyer, and H. Zeng, “A four-mode model for efficient fault-tolerant mixed-criticality systems,” in *Conference on Design, Automation and Test in Europe (DATE)*, 2016.

- [215] S. Azimi, B. Du, and L. Sterpone, “On the prediction of radiation-induced SETs in flash-based FPGAs,” *Microelectronics Reliability*, Elsevier, 2016.
- [216] H. Zhang, L. Bauer, M. A. Kochte, E. Schneider, H.-J. Wunderlich, and J. Henkel, “Aging resilience and fault tolerance in runtime reconfigurable architectures,” *IEEE Transactions on Computers*, 2016.
- [217] F. Siegle, T. Vladimirova, J. Ilstad, and O. Emam, “Mitigation of radiation effects in SRAM-based FPGAs for space applications,” *ACM Computing Surveys*, 2015.
- [218] N. T. H. Nguyen, “Repairing FPGA configuration memory errors using dynamic partial reconfiguration,” Ph.D. dissertation, The University of New South Wales, 2017.
- [219] G. Rieke, M. Ressler, J. E. Morrison, L. Bergeron, P. Bouchet, M. García-Marín, T. Greene, M. Regan, K. Sukhatme, and H. Walker, “The mid-infrared instrument for the james webb space telescope, VII: the MIRI detectors,” *Publications of the Astronomical Society of the Pacific*, vol. 127, no. 953, p. 665, 2015.
- [220] D. Evans and M. Merri, “OPS-SAT: An ESA nanosatellite for accelerating innovation in satellite control,” in *SpaceOps Conference*. ESA, 2014.
- [221] H. Kayal, F. Baumann, K. Briess, and S. Montenegro, “Beesat: A pico satellite for the on orbit verification of micro wheels,” in *IEEE International Conference on Recent Advances in Space Technologies (RAST)*. IEEE, 2007, pp. 497–502.
- [222] S. Fitzsimmons, “Reliable software updates for on-orbit CubeSat satellites,” Ph.D. dissertation, Master Thesis, California Polytechnic State University, 2012, 2012.
- [223] S. Busch and K. Schilling, “UWE-3: a modular system design for the next generation of very small satellites,” in *Small Satellites Systems and Services—The 4S Symposium*, ESA Press, 2012.
- [224] A. Corporation, “Arria GX device handbook, volume 2: Jam STAPL,” 2008.
- [225] S. M. Guertin, “CubeSat and mobile processors,” in *NASA Electronics Technology Workshop*, 2015, pp. 23–26.
- [226] A. Pirovano, A. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, “Scaling analysis of phase-change memory technology,” in *International Electron Devices Meeting (IEDM)*. IEEE, 2003, pp. 29–6.
- [227] Y. Huai, “Spin-transfer torque MRAM (STT-MRAM): Challenges and prospects,” *AAPPS Bulletin, Association of Asia Pacific Physical Societies*, vol. 18, no. 6, pp. 33–40, 2008.
- [228] K. Suzuki, D. Tonien, K. Kurosawa, and K. Toyota, “Birthday paradox for multi-collisions,” in *International Conference on Information Security and Cryptology (ICISC)*, Springer, 2006.
- [229] S. Wicker and V. Bhargava, *Reed-Solomon codes and their applications*. John Wiley & Sons, 1999.

- [230] F. Irom *et al.*, “SEEs and TID results of highly scaled flash memories,” in *IEEE Radiation Effects Data Workshop (REDW)*, 2013.
- [231] CNES, “Utilisation DSP FPGA Xilinx Spartan 6 pour application spatiale,” 2013, dCT/AQ/EC-2012/0019591.
- [232] ——, “Fiabilité d’un module de processing haute performance à base de FPGA CMP Xilinx Spartan 6,” 2014, dCT/AQ/EC-2014/01646.
- [233] ——, “Spécification technique de besoin pour évaluation en dose cumulée d’un FPGA CMP en Co60,” 2015, dCT/AQ/EC-2015/01158.
- [234] J. Heiner, B. Sellers, M. Wirthlin, and J. Kalb, “FPGA partial reconfiguration via configuration scrubbing,” in *International Conference on Field Programmable Logic and Applications (FPL)*. IEEE, 2009, pp. 99–104.
- [235] J. D. Corbett, “The xilinx isolation design flow for fault-tolerant systems,” *Xilinx White Paper WP412*, vol. 53, 2012.
- [236] L. Sterpone and B. Du, “SET-PAR: place and route tools for the mitigation of single event transients on flash-based FPGAs,” in *Applied Reconfigurable Computing*. Springer, 2015, pp. 129–140.
- [237] F. Kastensmidt and P. Rech, *FPGAs and Parallel Architectures for Aerospace Applications: Soft Errors and Fault-Tolerant Design*. Springer, 2016.
- [238] M. Wirthlin, “High-reliability FPGA-based systems: space, high-energy physics, and beyond,” *Proceedings of the IEEE*, vol. 103, no. 3, 2015.
- [239] M. Ebrahimi, P. M. B. Rao, R. Seyyedi, and M. B. Tahoori, “Low-cost multiple bit upset correction in SRAM-based FPGA configuration frames,” *IEEE Transactions on VLSI Systems*, 2016.
- [240] F. Rittner, M. Ristic, R. Glein, and A. Heuberger, “Automated test procedure to detect permanent faults inside SRAM-based FPGAs,” in *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*. IEEE, 2017.
- [241] U. Martinez-Corral and K. Basterretxea, “A fully configurable and scalable neural coprocessor ip for soc implementations of machine learning applications,” in *NASA/ESA Conference on Adaptive Hardware and Systems (AHS)*. IEEE, 2017.
- [242] A. Stoddard, A. Gruwell, P. Zabriskie, and M. J. Wirthlin, “A hybrid approach to FPGA configuration scrubbing,” *IEEE Transactions on Nuclear Science*, 2017.
- [243] F. Siegle, T. Vladimirova, J. Ilstad, and O. Emam, “Availability analysis for satellite data processing systems based on SRAM FPGAs,” *IEEE Transactions on Aerospace and Electronic Systems*, vol. 52, no. 3, pp. 977–989, 2016.
- [244] S. Wang, Y. Higami, H. Takahashi, M. Sato, M. Katsu, and S. Sekiguchi, “Testing of interconnect defects in memory based reconfigurable logic device (MRLD),” in *IEEE Asian Test Symposium (ATS)*, 2017.
- [245] A. Guerrieri, B. Belhadj, P. Lombardi, P. Ienne, and S. Kashani Akhavan, “FPGA based multithreading for on-board processing,” in *Space FPGA Users Workshop*, 2018, ESA/CNES.

- [246] A. K. Singh, M. Shafique, A. Kumar, and J. Henkel, “Mapping on multi/many-core systems: survey of current and emerging trends,” in *ACM/EDAC/IEEE Design Automation Conference (DAC)*. ACM, 2013.
- [247] E. Carvalho, N. Calazans, and F. Moraes, “Heuristics for dynamic task mapping in NoC-based heterogeneous MPSoCs,” in *IEEE/IFIP International Workshop on Rapid System Prototyping (RSP)*. IEEE, 2007.
- [248] RTEMS Development Team, “The real-time executive for multiprocessor systems RTOS,” project website: www.rtems.org.
- [249] J. Bouwmeester and J. Guo, “Survey of worldwide pico-and nanosatellite missions, distributions and subsystem technology,” *Acta Astronautica*, Elsevier, vol. 67, no. 7, 2010.
- [250] L. Z. Scheick, S. M. Guertin, and G. M. Swift, “Analysis of radiation effects on individual DRAM cells,” *IEEE Transactions on Nuclear Science*, 2000.
- [251] A. A. Hwang, I. A. Stefanovici, and B. Schroeder, “Cosmic rays don’t strike twice: understanding the nature of DRAM errors and the implications for system design,” *ACM SIGPLAN Notices*, 2012.
- [252] D. Dopson, “SoftECC: A system for software memory integrity checking,” Ph.D. dissertation, Massachusetts Institute of Technology, 2005.
- [253] R. Goodman and M. Sayano, “On-chip ECC for multi-level random access memories,” in *IEEE/CAM Information Theory Workshop at Cornell*. IEEE, 1989.
- [254] D. Bhattacharryya and S. Nandi, “An efficient class of SEC-DED-AUED codes,” in *International Symposium on Parallel Architectures, Algorithms and Networks (I-SPAN)*. IEEE, 1997.
- [255] A. Samaras, F. Bezerra, E. Lorfevre, and R. Ecoffet, “Carmen-2: In flight observation of non destructive single event phenomena on memories,” in *Conference on Radiation and its Effects on Components and Systems (RADECS)*. IEEE, 2011.
- [256] Y. You and J. Hayes, “A self-testing dynamic RAM chip,” *IEEE Transactions on Electron Devices*, 1985.
- [257] D. Callaghan, “Self-testing RAM system and method,” 2008, US Patent 7,334,159.
- [258] J. Foley, “Adaptive memory scrub rate,” 2012, US Patent 8,255,772.
- [259] M. Stringfellow, N. Leveson, and B. Owens, “Safety-driven design for software-intensive aerospace and automotive systems,” *Proceedings of the IEEE*, vol. 98, no. 4, pp. 515–525, 2010.
- [260] K. Ryu, E. Shin, and V. Mooney, “A comparison of five different multiprocessor soc bus architectures,” in *Euromicro Symposium on Digital Systems Design*. IEEE, 2001.
- [261] D. McComas, “NASA/GSFC’s flight software core flight system,” *NASA*, 2012.

- [262] J. Williams and N. Bergmann, "Reconfigurable linux for spaceflight applications," *Single Event Effects Symposium (SEE) & Military and Aerospace Programmable Logic Devices (MAPLD)*, 2004.
- [263] D. Atienza, J. Mendias, S. Mamagkakis, D. Soudris, and F. Catthoor, "Systematic dynamic memory management design methodology for reduced memory footprint," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 11, no. 2, pp. 465–489, 2006.
- [264] J. Saleh, D. Hastings, and D. Newman, "Weaving time into system architecture: satellite cost per operational day and optimal design lifetime," *Acta Astronautica, Elsevier*, vol. 54, no. 6, pp. 413–431, 2004.
- [265] M. Baker, M. Shah, D. Rosenthal, M. Roussopoulos, P. Maniatis, T. Giuli, and P. Bungale, "A fresh look at the reliability of long-term digital storage," in *ACM SIGOPS Operating Systems Review*, vol. 40. ACM, 2006, pp. 221–234.
- [266] J. Engel and R. Mertens, "LogFS-finally a scalable flash file system," in *International Linux System Technology Conference (LinuxCon)*. Linux Foundation, 2005.
- [267] S. Qiu and N. Reddy, "NVMFS: A hybrid file system for improving random write in NAND-flash SSD," in *Symposium on Mass Storage Systems and Technologies (MSST)*. IEEE, 2013.
- [268] W. Liangzhu, "The investigation of JFFS2 storage," *Microcomputer Information*, vol. 8, p. 030, 2008.
- [269] N. K. Edel, D. Tuteja, E. L. Miller, and S. A. Brandt, "MRAMFS: A compressing file system for non-volatile RAM," in *Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunications Systems (MASCOTS)*. IEEE, 2004, pp. 596–603.
- [270] M. Stornelli, "Protected and persistent RAM filesystem," pramfs.sourceforge.net.
- [271] J. Hulbert, "The Advanced XIP file system," in *Linux Symposium (OLS)*. Linux Foundation, 2008, p. 211.
- [272] D. Nguyen and F. Irom, "Radiation effects on MRAM," in *Conference on Radiation and its Effects on Components and Systems (RADECS)*. IEEE, 2007.
- [273] M. Elghefari and S. McClure, "Radiation effects assessment of MRAM devices," NASA/JPL, Tech. Rep., 2008.
- [274] M. Cassel, D. Walter, H. Schmidt, F. Gliem, H. Michalik, M. Stähle, K. Vögele, and P. Roos, "NAND-flash memory technology in mass memory systems for space applications," in *Eurospace Data Systems In Aerospace (DASIA)*, 2008.
- [275] H. Herpel, M. Stähle, U. Lonsdorfer, and N. Binzer, "Next generation mass memory architecture," in *Eurospace Data Systems In Aerospace (DASIA)*, 2010.
- [276] S. Suzuki and K. Shin, "On memory protection in real-time os for small embedded systems," in *Workshop Real-Time Computing Systems and Applications (RTCSA)*. IEEE, 1997.

- [277] S. Su and E. DuCasse, “A hardware redundancy reconfiguration scheme for tolerating multiple module failures,” *IEEE Transactions on Computers*, vol. 100, no. 3, pp. 254–258, 1980.
- [278] B. Cagno, J. Elliott, R. Kubo, and G. Lucas, “Verifying data integrity of a non-volatile memory system during data caching process,” US Patent 8,037,380.
- [279] V. Prabhakaran, A. Arpacı-Dusseau, and R. Arpacı-Dusseau, “Analysis and evolution of journaling file systems.” in *USENIX Annual Technical Conference*, 2005.
- [280] M. Cropper *et al.*, “VIS: the visible imager for Euclid,” in *SPIE Astronomical Telescopes + Instrumentation*, 2012.
- [281] ESA/SRE, *JUICE Definition Study Report*. ESA, September 2014.
- [282] ——, *EUCLID Definition Study Report*. ESA, July 2011.
- [283] K. F. Strauss and T. Daud, “Overview of radiation tolerant unlimited write cycle non-volatile memory,” in *IEEE Aerospace Conference*, 2000.
- [284] A. P. Ferreira, B. Childers, R. Melhem, D. Mossé, and M. Yousif, “Using PCM in next-generation embedded space applications,” in *RTAS*. IEEE, 2010.
- [285] N. Gupta, B. Vermeire, H. Barnaby, M. Goksel, E. Li, and D. Czajkowski, “Design of a 1 Gb radiation hardened NAND flash memory,” in *Non-Volatile Memory Technology Symposium*. IEEE, 2007.
- [286] S. Suzuki, Y. Deguchi, T. Nakamura, K. Mizoguchi, and K. Takeuchi, “Error elimination ECC by horizontal error detection and vertical-LDPC ECC to increase data-retention time by 230% and acceptable bit-error rate by 90% for 3D-NAND flash SSDs,” in *IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2018, pp. P–MY.
- [287] F. Irom, D. N. Nguyen, M. L. Underwood, and A. Virtanen, “Effects of scaling in SEE and TID response of high density NAND flash memories,” *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3329–3335, 2010.
- [288] S. Zertal, “A reliability enhancing mechanism for a large flash embedded satellite storage system,” in *IEEE International Conference on Systems (ICONS)*, 2008.
- [289] B. Kroth and S. Yang, “Checksumming RAID,” 2010, university of Wisconsin-Madison, unpublished manuscript.
- [290] E. M. Kurtas, A. V. Kuznetsov, and I. Djurdjevic, “System perspectives for the application of structured LDPC codes to data storage,” *IEEE Transactions on Magnetics*, vol. 42, 2006.
- [291] K. S. Andrews, D. Divsalar, S. Dolinar, J. Hamkins, C. R. Jones, and F. Polllara, “The development of Turbo and LDPC codes for deep-space applications,” *Proceedings of the IEEE*, vol. 95, no. 11, 2007.
- [292] M. Lentmaier, A. Sridharan, D. J. Costello, and K. S. Zigangirov, “Iterative decoding threshold analysis for LDPC convolutional codes,” *IEEE Transactions on Information Theory*, 2010.

- [293] T. Morita, M. Ohta, and T. Sugawara, “Efficiency of short LDPC codes combined with long reed-solomon codes for magnetic recording channels,” *IEEE Transactions on Magnetics*, vol. 40, no. 4, pp. 3078–3080, 2004.
- [294] Z. Shi, C. Fu, and S. Li, “Serial concatenation and joint iterative decoding of LDPC codes and Reed-Solomon codes,” *National Laboratory of Communication, UESTC, Chengdu, China*, vol. 610054, 2006.
- [295] P. Sobe, “Reliability modeling of fault-tolerant storage system-covering MDS-codes and regenerating codes,” in *International Conference on Architecture of Computing Systems (ARCS)*, 2013.
- [296] M. Nowak, S. Lacour, A. Crouzier, L. David, V. Lapeyrère, and G. Schworer, “Short life and abrupt death of picsat, a small 3u CubeSat dreaming of exoplanet detection,” in *Space Telescopes and Instrumentation 2018: Optical, Infrared, and Millimeter Wave*, vol. 10698. International Society for Optics and Photonics, 2018, p. 1069821.
- [297] D. S. Lee, G. R. Allen, G. Swift, M. Cannon, M. Wirthlin, J. S. George, R. Koga, and K. Huey, “Single-event characterization of the 20 nm Xilinx Kintex Ultrascale field-programmable gate array under heavy ion irradiation,” in *IEEE Radiation Effects Data Workshop (REDW)*. IEEE, 2015.
- [298] M. Glorieux, A. Evans, T. Lange, A.-D. In, D. Alexandrescu, C. Boatella-Polo, R. G. Alifa, M. Tali, C. U. Ortega, M. Kastriotou *et al.*, “Single-event characterization of Xilinx UltraScale+ MPSoC under standard and ultra-high energy heavy-ion irradiation,” in *IEEE Nuclear & Space Radiation Effects Conference (NSREC)*. IEEE, 2018, pp. 1–5.
- [299] D. S. Lee, M. King, W. Evans, M. Cannon, A. Pérez-Celis, J. Anderson, M. Wirthlin, and W. Rice, “Single-event characterization of 16 nm FinFET Xilinx UltraScale+ devices with heavy ion and neutron irradiation,” in *IEEE Nuclear & Space Radiation Effects Conference (NSREC)*. IEEE, 2018.
- [300] R. Natella, D. Cotroneo, and H. S. Madeira, “Assessing dependability with software fault injection: A survey,” *ACM Computing Surveys*, 2016.
- [301] B. Sangchoolie, R. Johansson, and J. Karlsson, “Light-weight techniques for improving the controllability and efficiency of isa-level fault injection tools,” in *IEEE Pacific Rim International Symposium on Dependable Computing (PRDC)*. IEEE, 2017.
- [302] D. Cotroneo, A. Lanzaro, R. Natella, and R. Barbosa, “Experimental analysis of binary-level software fault injection in complex software,” in *European Dependable Computing Conference (EDCC)*. IEEE, 2012.
- [303] R. Natella, D. Cotroneo, J. A. Duraes, and H. S. Madeira, “On fault representativeness of software fault injection,” *IEEE Transactions on Software Engineering*, vol. 39, no. 1, pp. 80–96, 2013.
- [304] L. Leem, H. Cho, J. Bau, Q. A. Jacobson, and S. Mitra, “ERSA: Error resilient system architecture for probabilistic applications,” in *Conference on Design, Automation and Test in Europe (DATE)*. EDAA, 2010.

- [305] R. Amarnath, S. N. Bhat, P. Munk, and E. Thaden, “A fault injection approach to evaluate soft-error dependability of system calls,” in *IEEE International Symposium on Software Reliability Engineering Workshops (ISSREW)*. IEEE, 2018, pp. 71–76.
- [306] H. Schirmeier, M. Hoffmann, C. Dietrich, M. Lenz, D. Lohmann, and O. Spinczyk, “FAIL: An open and versatile fault-injection framework for the assessment of software-implemented hardware fault tolerance,” in *European Dependable Computing Conference (EDCC)*. IEEE, 2015.
- [307] J. Isaza-González, A. Serrano-Cases, F. Restrepo-Calle, S. Cuenca-Asensi, and A. Martínez-Álvarez, “Dependability evaluation of cots microprocessors via on-chip debugging facilities,” in *IEEE Latin American Test Symposium (LATST)*, 2016.
- [308] D. Cozzi, “Run-time reconfigurable, fault-tolerant FPGA systems for space applications,” Ph.D. dissertation, Universität Bielefeld, 2016.
- [309] M. Alderighi, F. Casini, S. D’Angelo, S. Pastore, G. Sechi, and R. Weigand, “Evaluation of single event upset mitigation schemes for SRAM based FPGAs using the FLIPPER fault injection platform,” in *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*. IEEE, 2007.
- [310] W. Mansour and R. Velazco, “An automated SEU fault-injection method and tool for HDL-based designs,” *IEEE Transactions on Nuclear Science*, 2013.
- [311] D. Cotroneo and R. Natella, “Software fault injection for software certification,” *IEEE Security & Privacy*, 2013.
- [312] M. Kooli, P. Benoit, G. Di Natale, L. Torres, and V. Sieh, “Fault injection tools based on virtual machines,” in *Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC)*. IEEE, 2014.
- [313] A. Höller, G. Schönfelder, N. Kajtazovic, T. Rauter, and C. Kreiner, “FIES: a fault injection framework for the evaluation of self-tests for COTS-based safety-critical systems,” in *International Microprocessor Test and Verification Workshop (MTV)*. IEEE, 2014.
- [314] J. Power, J. Hestness, M. S. Orr, M. D. Hill, and D. A. Wood, “gem5-gpu: A heterogeneous cpu-gpu simulator,” *IEEE Computer Architecture Letters*, vol. 14, no. 1, pp. 34–36, 2015.
- [315] P. Lisherness and K.-T. T. Cheng, “SCEMIT: A SystemC error and mutation injection tool,” in *Design Automation Conference (DAC)*. ACM, 2010.
- [316] R. Natella, S. Winter, D. Cotroneo, and N. Suri, “Analyzing the effects of bugs on software interfaces,” *IEEE Transactions on Software Engineering*, 2018.
- [317] D. Sinclair and J. Dyer, “Radiation effects and cots parts in smallsats,” in *AIAA/USU Conference on Small Satellites (SmallSat)*, 2013.
- [318] R. L. Pease, A. H. Johnston, and J. L. Azarewicz, “Radiation testing of semiconductor devices for space electronics,” *Proceedings of the IEEE*, vol. 76, no. 11, pp. 1510–1526, 1988.

- [319] M. A. McMahan, E. Blackmore, E. W. Cascio, C. Castaneda, B. von Przewoski, and H. Eisen, “Standard practice for dosimetry of proton beams for use in radiation effects testing of electronics,” in *IEEE Radiation Effects Data Workshop (REDW)*. IEEE, 2008, pp. 135–141.
- [320] V. Sridharan and D. R. Kaeli, “Using hardware vulnerability factors to enhance avf analysis,” in *ACM SIGARCH Computer Architecture News*, vol. 38, no. 3. ACM, 2010, pp. 461–472.
- [321] M. Maniatakos, M. K. Michael, and Y. Makris, “Investigating the limits of avf analysis in the presence of multiple bit errors,” in *IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS)*. IEEE, 2013, pp. 49–54.
- [322] X. Li and D. Yeung, “Application-level correctness and its impact on fault tolerance,” in *International Symposium on High Performance Computer Architecture (HPCA)*. IEEE, 2007.
- [323] A. o. Velasco, “A hardening approach for the scheduler’s kernel data structures,” in *International Conference on Architecture of Computing Systems (ARCS)*, 2017.
- [324] A. Serrano-Cases, Y. Morilla, P. Martín-Holgado, S. Cuenca-Asensi, and A. Martínez-Álvarez, “Automatic compiler-guided reliability improvement of embedded processors under proton irradiation,” in *Conference on Radiation and its Effects on Components and Systems (RADECS)*. IEEE, 2018.
- [325] A. Serrano-Cases, J. Isaza-González, S. Cuenca-Asensi, and A. Martínez-Álvarez, “On the influence of compiler optimizations in the fault tolerance of embedded systems,” in *IEEE International Symposium on On-Line Testing and Robust System Design (IOLTS)*. IEEE, 2016.
- [326] F. M. Lins, L. A. Tambara, F. L. Kastensmidt, and P. Rech, “Register file criticality and compiler optimization effects on embedded microprocessor reliability,” *IEEE Transactions on Nuclear Science*, 2017.
- [327] P. Larsen, A. Homescu, S. Brunthaler, and M. Franz, “Sok: Automated software diversity,” in *IEEE Symposium on Security and Privacy (SP)*. IEEE, 2014, pp. 276–291.
- [328] P. Meloni *et al.*, “System adaptivity and fault-tolerance in NoC-based MPSoCs: the MADNESS project approach,” in *IEEE DSD*, 2012.
- [329] N. K. R. Beechu, V. M. Harishchandra, and N. K. Y. Balachandra, “Hardware implementation of fault tolerance NoC core mapping,” *Springer Telecommunication Systems*, 2017.
- [330] N. Katta, H. Zhang, M. Freedman, and J. Rexford, “Ravana: Controller fault-tolerance in software-defined networking,” in *ACM SIGCOMM*. ACM, 2015.
- [331] Z. K. Baker and H. M. Quinn, “Design and test of Xilinx embedded ECC for MicroBlaze processors,” in *IEEE Radiation Effects Data Workshop (REDW)*. IEEE, 2016, pp. 1–7.

- [332] Z. Zhang, Z. Lei, Z. Yang, X. Wang, B. Wang, J. Liu, Y. En, H. Chen, and B. Li, “Single event effects in COTS ferroelectric RAM technologies,” in *IEEE Radiation Effects Data Workshop (REDW)*. IEEE, 2015.
- [333] Y. Li, B. Nelson, and M. Wirthlin, “Synchronization techniques for crossing multiple clock domains in FPGA-based TMR circuits,” *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3506–3514, 2010.
- [334] J. Standeven, M. J. Colley, and D. Lyons, “Hardware voter for fault-tolerant transputer systems,” *Microprocessors and Microsystems*, Elsevier, vol. 13, no. 9, pp. 588–596, 1989.
- [335] A. T. Tai, S. N. Chau, and L. Alkalai, “COTS-based fault tolerance in deep space: Qualitative and quantitative analyses of a bus network architecture,” in *International Symposium on High-Assurance Systems Engineering (HASE)*. IEEE, 1999.
- [336] H. Kimm and M. Jarrell, “Controller area network for fault tolerant small satellite system design,” in *IEEE International Symposium on Industrial Electronics (ISIE)*. IEEE, 2014, pp. 81–86.
- [337] C. Wilson, J. MacKinnon, P. Gauvin, S. Sabogal, A. D. George, G. Crum, and T. Flatley, “μcsp: A diminutive, hybrid, space processor for smart modules and CubeSats,” in *AIAA/USU Conference on Small Satellites (SmallSat)*, 2016.
- [338] S. Parkes and P. Armbruster, “SpaceWire: a spacecraft onboard network for real-time communications,” in *IEEE-NPSS Real Time Conference (RT)*. IEEE, 2005.
- [339] H. Zimmermann, “OSI reference model—the ISO model of architecture for open systems interconnection,” *IEEE Transactions on communications*, 1980.
- [340] V. Gavrilut, B. Zarrin, P. Pop, and S. Samii, “Fault-tolerant topology and routing synthesis for IEEE time-sensitive networking,” in *International Conference on Real-Time Networks and Systems (RTNS)*. ACM, 2017.
- [341] G. J. Brebner, “Reconfigurable computing for high performance networking applications.” *ARC*, vol. 1, 2011.
- [342] J. Anderson, K. Bauer, A. Borga, H. Boterenbrood, H. Chen, K. Chen, G. Drake, M. Dönszelmann, D. Francis, D. Guest *et al.*, “Felix: a pcie based high-throughput approach for interfacing front-end and trigger electronics in the atlas upgrade framework,” *Journal of Instrumentation, IOP Publishing*, 2016.
- [343] M. Dreschmann, J. Heisswolf, M. Geiger, J. Becker, and M. HauBecker, “A framework for multi-FPGA interconnection using multi gigabit transceivers,” in *Symposium on Integrated Circuits and Systems Design (SBCCI)*. IEEE, 2015.
- [344] C. Carmichael, “Triple module redundancy design techniques for Virtex FPGAs,” *Xilinx Application Note XAPP197*, 2001.

- [345] A. Fedi, M. Ottavi, G. Furano, A. Bruno, R. Senesi, C. Andreani, and C. Cazzaniga, “High-energy neutrons characterization of a safety critical computing system,” in *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*. IEEE, 2017, pp. 1–4.
- [346] Á. B. de Oliveira, L. A. Tambara, and F. L. Kastensmidt, “Applying lockstep in dual-core ARM Cortex-A9 to mitigate radiation-induced soft errors,” in *IEEE Latin American Symposium on Circuits & Systems (LASCAS)*. IEEE, 2017.
- [347] R. V. Kshirsagar and R. M. Patrikar, “Design of a novel fault-tolerant voter circuit for TMR implementation to improve reliability in digital circuits,” *Microelectronics Reliability*, Elsevier, 2009.
- [348] M. Liu and B. H. Meyer, “Bounding error detection latency in safety critical systems with enhanced execution fingerprinting,” in *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*. IEEE, 2016.
- [349] E. Wachter, V. Fochi, F. Barreto, A. Amory, and F. Moraes, “A hierarchical and distributed fault tolerant proposal for NoC-based MPSoCs,” *IEEE Transactions on Emerging Topics in Computing*, 2016.
- [350] W. Liu, W. Zhang, X. Wang, and J. Xu, “Distributed sensor network-on-chip for performance optimization of soft-error-tolerant multiprocessor system-on-chip,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 4, pp. 1546–1559, 2016.
- [351] S. S. Sahoo, B. Veeravalli, and A. Kumar, “Cross-layer fault-tolerant design of real-time systems,” in *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*. IEEE, 2016.
- [352] E. Benton and E. Benton, “Space radiation dosimetry in low-earth orbit and beyond,” *Nuclear Instruments and Methods in Physics Research*, Elsevier, 2001.
- [353] V. Sridharan and D. Liberty, “A study of DRAM failures in the field,” in *Conference on High Performance Computing, Networking, Storage and Analysis (SC)*. IEEE, 2012.
- [354] P. Maillard, M. Hart, J. Barton, P. Chang, M. Welter, R. Le, R. Ismail, and E. Crabill, “Single-event upsets characterization & evaluation of Xilinx UltraScale soft error mitigation (SEM IP) tool,” in *IEEE Radiation Effects Data Workshop (REDW)*. IEEE, 2016, pp. 1–4.
- [355] C. Bolchini, A. Miele, and M. D. Santambrogio, “TMR and partial dynamic reconfiguration to mitigate SEU faults in FPGAs,” in *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*. IEEE, 2007, pp. 87–95.
- [356] G. Durrieu, G. Fohler, G. Gala, S. Girbal, D. G. Pérez, E. Noulard, C. Pagetti, and S. Pérez, “Dreams about reconfiguration and adaptation in avionics,” *Embedded Real Time Software and Systems Congress (ERTS)*, 2016.

- [357] M. Darvishi, Y. Audet, Y. Blaqui  re, C. Thibeault, and S. Pichette, “On the susceptibility of SRAM-based FPGA routing network to delay changes induced by ionizing radiation,” *IEEE Transactions on Nuclear Science*, 2019.
- [358] M. Payer, “Too much PIE is bad for performance,” *ETH Zurich Technical Report*, vol. 766, 2012.
- [359] J. W. Lee, M. C. Ng, and K. Asanovic, “Globally-synchronized frames for guaranteed quality-of-service in on-chip networks,” in *ACM SIGARCH Computer Architecture News*, vol. 36, no. 3. IEEE Computer Society, 2008, pp. 89–100.
- [360] TSMC’s industry-first and leading 7nm technology enters volume production. [Online]. Available: <https://www.tsmc.com/csr/en/update/innovationAndService/caseStudy/9/index.html>
- [361] S.-D. Kim, M. Guillorn, I. Lauer, P. Oldiges, T. Hook, and M.-H. Na, “Performance trade-offs in FinFET and gate-all-around device architectures for 7nm-node and beyond,” in *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*. IEEE, 2015, pp. 1–3.
- [362] Z. Zhang, Z. Zhan, D. Balasubramanian, X. Koutsoukos, and G. Karsai, “Triggering rowhammer hardware faults on arm: A revisit,” in *Workshop on Attacks and Solutions in Hardware Security*. ACM, 2018, pp. 24–33.