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Bibliography

[ABD08] J. H. Anderson, V. Bud, and U. C. Devi. An edf-based restricted-migration scheduling algorithm for multiprocessor soft real-time systems. *Real-Time Systems*, 38(2):85–131, 2 2008. doi:10.1007/s11241-007-9035-0.

[ABR+93] N. Audsley, A. Burns, M. Richardson, K. Tindell, and A. J. Wellings. Applying new scheduling theory to static priority pre-emptive scheduling. *Software Eng. J.*, 8:284–292(8), 1993.

[ABRW91] N. C. Audsley, A. Burns, M. M. Richardson, and A. J. Wellings. Hard real-time scheduling: The deadline-monotonic approach. In *Proceedings of 8th IEEE Workshop on Real-Time Operating Systems and Software*, pages 133–137, 1991.

[ARM] ARM. AMBA Specifications. URL: https://www.arm.com/products/system-ip/amba-specifications.php [cited June 8, 2016].

[AS04] K. Albers and F. Slomka. An event stream driven approximation for the analysis of real-time systems. In *Proceedings of the 16th Euromicro Conference on Real-Time Systems*, ECRTS '04, pages 187–195, Washington, DC, USA, 2004. IEEE Computer Society. URL: http://dx.doi.org/10.1109/ECRTS.2004.4, doi:10.1109/ECRTS.2004.4.

[AT06] B. Andersson and E. Tovar. Multiprocessor scheduling with few preemptions. In *Proceedings of the 12th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications*, RTCSA '06, pages 322–334. IEEE, 2006. doi:10.1109/RTCSA.2006.45.

[AXI] ARM Ltd., AMBA AXI Protocol - Version: 2.0 : Specification, 2010. http://www.arm.com.

[AY03] H. Aydin and Q. Yang. Energy-aware partitioning for multiprocessor real-time systems. In *Proceedings of the 17th International Symposium on Parallel and Distributed Processing*, IPDPS '03, pages 113.2–, Washington, DC, USA, 2003. IEEE Computer Society. URL: http://dl.acm.org/citation.cfm?id=838237.838347.

[Bam12] M. Bamakhrama, 2012. http://daedalus.liacs.nl/darts.

[BB04] D. Bertozzi and L. Benini. Xpipes: a network-on-chip architecture for gigascale systems-on-chip. *Circuits and Systems Magazine, IEEE*, 4(2):18–31, September 2004. URL: http://dx.doi.org/10.1109/mcas.2004.1330747, doi:10.1109/mcas.2004.1330747.

[BCPV96] S. K. Baruah, N. K. Cohen, C. G. Plaxton, and D. A. Varvel. Proportionate progress: A notion of fairness in resource allocation. *Algorithmica*, 15(6):600–625, 1996. doi:10.1007/BF01940883.

[BDM02] L. Benini and G. De Micheli. Networks on chips: A new soc paradigm. *Computer*, 35(1):70–78, January 2002. URL: http://dx.doi.org/10.1109/2.976921, doi:10.1109/2.976921.

[BELP96] G. Bilsen, M. Engels, R. Lauwereins, and J. Peperstraete. Cyclo-static dataflow. *IEEE Transactions on Signal Processing*, 44(2):397–408, 1996. doi:10.1109/78.485935.

[BF05] S. Baruah and N. Fisher. The partitioned multiprocessor scheduling of sporadic task systems. In *Proceedings of the 26th IEEE International Real-Time Systems Symposium*, RTSS '05, pages 321–329, Washington, DC, USA, 2005. IEEE Computer Society. URL: http://dx.doi.org/10.1109/RTSS.2005.40, doi:10.1109/RTSS.2005.40.

[BL13] D. Bui and E. A. Lee. Streamorph: A case for synthesizing energy-efficient adaptive programs using high-level abstractions. In *Proceedings of the Eleventh ACM International Conference on Embedded Software*, EMSOFT '13, pages 20:1–20:10, Piscataway, NJ, USA, 2013. IEEE Press. URL: http://dl.acm.org/citation.cfm?id=2555754.2555774.

[BMAB16] M. Bambagini, M. Marinoni, H. Aydin, and G. Buttazzo. Energy-aware scheduling for real-time systems: A survey. *ACM Trans. Embed. Comput. Syst.*, 15(1):7:1–7:34, January 2016. URL: http://doi.acm.org/10.1145/2808231, doi:10.1145/2808231.

[BMKdD13] B. Bodin, A. Munier-Kordon, and B. Dupont de Dinechin. Periodic Schedules for Cyclo-Static Dataflow. In *Proceedings of the 11th IEEE Symposium on Embedded Systems for Real-Time Multimedia*, ESTIMedia 2013, pages 105–114, 2013. doi:10.1109/ESTIMedia.2013.6704509.

[BMMKM10] M. Benazouz, O. Marchetti, A. Munier Kordon, and T. Michel. A new method for minimizing buffer sizes for cyclo-static dataflow graphs. In *Proceedings of the 8th IEEE Symposium on Embedded Systems for Real-Time Multimedia*, ESTIMedia 2010, pages 11–20, 2010.

[BRH90] S. K. Baruah, L. E. Rosier, and R. R. Howell. Algorithms and complexity concerning the preemptive scheduling of periodic, real-time tasks on one processor. *Real-Time Systems*, 2:301–324, 1990. doi:10.1007/BF01995675.

[BS11] M. Bamakhrama and T. Stefanov. Hard-real-time scheduling of data-dependent tasks in embedded streaming applications. In *Proceedings of the ninth ACM International Conference on Embedded Software*, EMSOFT '11, pages 195–204, New York, NY, USA, 2011. ACM. doi:10.1145/2038642.2038672.

[BS13] M. A. Bamakhrama and T. P. Stefanov. On the hard-real-time scheduling of embedded streaming applications. *Design Automation for Embedded Systems*, 17(2):221–249, 2013. URL: http://dx.doi.org/10.1007/s10617-012-9086-x, doi:10.1007/s10617-012-9086-x.

[BTM00] D. Brooks, V. Tiwari, and M. Martonosi. Wattch: A framework for architectural-level power analysis and optimizations. In *Proc. of ISCA*, pages 83–94, 2000.

[BTV12] A. Bouakaz, J.-P. Talpin, and J. Vitek. Affine Data-Flow Graphs for the Synthesis of Hard Real-Time Applications. In *Proceedings of the 12th International Conference on Application of Concurrency*

to System Design, ACSD '12, pages 183–192, Los Alamitos, CA, USA, 2012. IEEE Computer Society. doi:10.1109/ACSD.2012.16.

[BVC04] N. Banerjee, P. Vellanki, and K.S. Chatha. A power and performance model for network-on-chip architectures. In *Proc. of DATE - Volume 2*, 2004.

[BZNS12] M. A. Bamakhrama, J. Teddy Zhai, H. Nikolov, and T. Stefanov. A methodology for automated design of hard-real-time embedded streaming systems. In *Proceedings of the 15th Design, Automation Test in Europe Conference and Exhibition*, DATE 2012, pages 941–946, 2012. doi:10.1109/DATE.2012.6176632.

[BZZ04] A. Bona, V. Zaccaria, and R. Zafalon. System level power modeling and simulation of high-end industrial network-on-chip. In *Proc. of DATE - Volume 3*, 2004.

[C+10] X. Chen et al. Performance and power modeling in a multi-programmed multi-core environment. In *Proc. of DAC*, pages 813–818, 2010.

[CAC] HP Labs, CACTI. http://www.hpl.hp.com/research/cacti.

[CGJ96] E. G. Coffman, Jr., M. R. Garey, and D. S. Johnson. Approximation algorithms for bin packing: A survey. In Dorit S. Hochbaum, editor, *Approximation algorithms for NP-hard problems*, pages 46–93. PWS Publishing Co., Boston, MA, USA, 1996.

[CKR14] A. Colin, A. Kandhalu, and R. Rajkumar. Energy-efficient allocation of real-time applications onto heterogeneous processors. In *RTSCA*, 2014.

[CRJ06] H. Cho, B. Ravindran, and E. D. Jensen. An optimal real-time scheduling algorithm for multiprocessors. In *Proceedings of the 27th IEEE International Real-Time Systems Symposium*, RTSS '06, pages 101–110, Washington, DC, USA, 2006. IEEE Computer Society. URL: http://dx.doi.org/10.1109/RTSS.2006.10, doi:10.1109/RTSS.2006.10.

[DB11] R. I. Davis and A. Burns. A survey of hard real-time scheduling for multiprocessor systems. *ACM Computing Surveys*, 43(4):35:1–35:44, 2011. doi:10.1145/1978802.1978814.

[DK89] M. L. Dertouzos and A. Ka-Lau Mok. Multiprocessor online scheduling of hard-real-time tasks. *IEEE Transactions on Software Engineering*, 15(12):1497–1506, 1989. doi:10.1109/32.58762.

[DSB+13] M. Damavandpeyma, S. Stuijk, T. Basten, M. Geilen, and H. Corporaal. Throughput-constrained dvfs for scenario-aware dataflow graphs. In *RTAS*, 2013.

[EBSA+11] H. Esmaeilzadeh, E. Blem, R. St. Amant, K. Sankaralingam, and D. Burger. Dark silicon and the end of multicore scaling. In *Proceedings of the 38th Annual International Symposium on Computer Architecture*, ISCA '11, pages 365–376, New York, NY, USA, 2011. ACM. URL: http://doi.acm.org/10.1145/2000064.2000108, doi:10.1145/2000064.2000108.

[EJ09] C. Ebert and C. Jones. Embedded Software: Facts, Figures, and Future. *IEEE Computer*, 42(4):42–52, 2009. doi:10.1109/MC.2009.118.

[Fea96a] P. Feautrier. Automatic Parallelization in the Polytope Model. In Guy-René Perrin and Alain Darte, editors, *The Data Parallel Programming Model: Foundations, HPF Realization, and Scientific Applications*, volume 1132, pages 79–103. Springer Berlin Heidelberg, 1996. doi:10.1007/3-540-61736-1_44.

[Fea96b] P. Feautrier. Automatic parallelization in the polytope model. In *The Data Parallel Programming Model*. Springer-Verlag, 1996.

[Fis07] N. Fisher. *The multiprocessor real-time scheduling of general task systems*. PhD thesis, Department of Computer Science, The University of North Carolina at Chapel Hill, Chapel Hill, NC., 2007.

[FKBS11] S. M. Farhad, Y. Ko, B. Burgstaller, and B. Scholz. Orchestration by approximation: Mapping stream programs onto multicore architectures. In *Proceedings of the Sixteenth International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS XVI, pages 357–368, New York, NY, USA, 2011. ACM. URL: http://doi.acm.org/10.1145/1950365.1950406, doi:10.1145/1950365.1950406.

[fSI] International Technology Roadmap for Semiconductors (ITRS). ITRS Reports. URL: http://www.itrs2.net/itrs-reports.html [cited June 12, 2016].

[GB14] M. Grant and S. Boyd. CVX: Matlab software for disciplined convex programming, ver. 2.1, 2014.

[GDR05] K. Goossens, J. Dielissen, and A. Rădulescu. Æthereal Network on Chip: Concepts, Architectures, and Implementations. *IEEE Design and Test of Computers*, 22(5):414–421, 2005. doi:10.1109/MDT.2005.99.

[GGS+06] A. H. Ghamarian, M. C. W. Geilen, S. Stuijk, T. Basten, B. D. Theelen, M. R. Mousavi, A. J. M. Moonen, and M. J. G. Bekooij. Throughput analysis of synchronous data flow graphs. In *Proceedings of the Sixth International Conference on Application of Concurrency to System Design*, ACSD '06, pages 25–36, Washington, DC, USA, 2006. IEEE Computer Society. URL: http://dx.doi.org/10.1109/ACSD.2006.33, doi:10.1109/ACSD.2006.33.

[GHP+09] A. Gerstlauer, C. Haubelt, A. D. Pimentel, T. P. Stefanov, D. D. Gajski, and J. Teich. Electronic System-Level Synthesis Methodologies. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 28(10):1517–1530, 2009. doi:10.1109/TCAD.2009.2026356.

[GJ79] M. R. Garey and D. S. Johnson. *Computers and Intractability: A Guide to the Theory of NP-Completeness*. WH Freeman & Co., New York, NY, USA, 1979.

[Gre11] P. Greenhalgh. Big.LITTLE processing with ARM Cortex-A15 & Cortex-A7, 2011.

[HA06] P. Holman and J. H. Anderson. Group-based Pfair scheduling. *Real-Time Systems*, 32(1–2):125–168, 2006. doi:doi:10.1007/s11241-006-4687-8.

[HGWB13] J. P. H. M. Hausmans, S. J. Geuns, M. H. Wiggers, and M. J.G. Bekooij. Two parameter workload characterization for improved dataflow analysis accuracy. In *Proceedings of the IEEE 19th Real-Time and Embedded Technology and Applications*

Symposium, RTAS '13, pages 117–126, Los Alamitos, CA, USA, 2013. IEEE Computer Society. doi:10.1109/RTAS.2013.6531085.

[HLF+11] C.-W. Hsu, J.-L. Liao, S.-C. Fang, C.-C. Weng, S.-Y. Huang, W.-T. Hsieh, and J.-C. Yeh. Powerdepot: Integrating ip-based power modeling with esl power analysis for multi-core soc designs. In *Proceedings of the 48th Design Automation Conference*, DAC '11, pages 47–52, New York, NY, USA, 2011. ACM. URL: http://doi.acm.org/10.1145/2024724.2024736, doi:10.1145/2024724.2024736.

[HM07] S. Herbert and D. Marculescu. Analysis of dynamic voltage/frequency scaling in chip-multiprocessors. In *Proceedings of the 2007 International Symposium on Low Power Electronics and Design*, ISLPED '07, pages 38–43, New York, NY, USA, 2007. ACM. URL: http://doi.acm.org/10.1145/1283780.1283790, doi:10.1145/1283780.1283790.

[HMGM13] P. Huang, O. Moreira, K. Goossens, and A. Molnos. Throughput-constrained voltage and frequency scaling for real-time heterogeneous multiprocessors. In *Proceedings of the 28th Annual ACM Symposium on Applied Computing*, SAC '13, pages 1517–1524, New York, NY, USA, 2013. ACM. URL: http://doi.acm.org/10.1145/2480362.2480645, doi:10.1145/2480362.2480645.

[HNP+15] S. Holmbacka, E. Nogues, M. Pelcat, S. Lafond, D. Menard, and J. Lilius. Energy-awareness and performance management with parallel dataflow applications. *J. of Signal Processing Systems*, pages 1–16, 2015.

[HP06] J. L. Hennessy and D. A. Patterson. *Computer Architecture, Fourth Edition: A Quantitative Approach*. Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, 2006.

[IBM12] IBM ILOG CPLEX Optimization Studio V12.4, 2012.

[Int11] The International Technology Roadmap for Semiconductors (ITRS), System Drivers, 2011. Available on: http://www.itrs.net.

[Joh74] D. S. Johnson. Fast algorithms for bin packing. *Journal of Computer and System Sciences*, 8(3):272–314, 1974. doi:10.1016/S0022-0000(74)80026-7.

[JTW05] A. Jerraya, H. Tenhunen, and W. Wolf. Multiprocessor Systems-on-Chips. *IEEE Computer*, 38(7):36–40, 2005. doi:10.1109/MC.2005.231.

[Kah13] A. B. Kahng. The itrs design technology and system drivers roadmap: Process and status. In *Proceedings of the 50th Annual Design Automation Conference*, DAC '13, pages 34:1–34:6, New York, NY, USA, 2013. ACM. URL: http://doi.acm.org/10.1145/2463209.2488776, doi:10.1145/2463209.2488776.

[KLPS09] A. B. Kahng, B. Li, L.-S. Peh, and K. Samadi. Orion 2.0: A fast and accurate noc power and area model for early-stage design space exploration. In *Proc. of DATE*, pages 423–428, 2009.

[KM08] M. Kudlur and S. Mahlke. Orchestrating the execution of stream programs on multicore platforms. In *Proceedings of the 29th ACM SIGPLAN Conference on Programming Language Design and Implementation*, PLDI '08, pages 114–124, New York, NY, USA, 2008. ACM. URL: http://doi.acm.org/10.1145/1375581.1375596, doi:10.1145/1375581.1375596.

[KMN+00] K.and Keutzer, S. Malik, A. R. Newton, J. M. Rabaey, and A. Sangiovanni-Vincentelli. System-level design: orthogonalization of concerns and platform-based design. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 19(12):1523–1543, 2000. doi:10.1109/43.898830.

[KS97] A. Khemka and R.K. Shyamasundar. An optimal multiprocessor real-time scheduling algorithm. *J. Parallel Distrib. Comput.*, 43(1):37–45, May 1997. URL: http://dx.doi.org/10.1006/jpdc.1997.1327, doi:10.1006/jpdc.1997.1327.

[KY07] S. Kato and N. Yamasaki. Real-time scheduling with task splitting on multiprocessors. In *Proceedings of the 13th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications*, RTCSA '07, pages 441–450. IEEE, 2007. doi:10.1109/RTCSA.2007.61.

[LB03] G. Lipari and E. Bini. Resource partitioning among real-time applications. In *Proceedings of 15th the Euromicro Conference on Real-Time Systems*, ECRTS '03, pages 151–158, 2003.

[Lee09] W. Y. Lee. Energy-saving dvfs scheduling of multiple periodic real-time tasks on multi-core processors. In *Proceedings of the 2009 13th IEEE/ACM International Symposium on Distributed Simulation and Real Time Applications*, DS-RT '09, pages 216–223, Washington, DC, USA, 2009. IEEE Computer Society. URL: http://dx.doi.org/10.1109/DS-RT.2009.12, doi:10.1109/DS-RT.2009.12.

[Leu89] J. Y. T. Leung. A new algorithm for scheduling periodic, real-time tasks. *Algorithmica*, 4(1):209–219, 1989. URL: http://dx.doi.org/10.1007/BF01553887, doi:10.1007/BF01553887.

[LJSM04] J. Laurent, N. Julien, E. Senn, and E. Martin. Functional level power analysis: An efficient approach for modeling the power consumption of complex processors. In *Proceedings of the Conference on Design, Automation and Test in Europe - Volume 1*, DATE '04, pages 10666–, Washington, DC, USA, 2004. IEEE Computer Society. URL: http://dl.acm.org/citation.cfm?id=968878.968987.

[LL73] C. L. Liu and J. W. Layland. Scheduling Algorithms for Multiprogramming in a Hard-Real-Time Environment. *Journal of the ACM*, 20(1):46–61, 1973. doi:10.1145/321738.321743.

[LM87] E. A. Lee and D. G. Messerschmitt. Synchronous data flow. *Proceedings of the IEEE*, 75(9):1235–1245, 1987. doi:10.1109/PROC.1987.13876.

[LPB04] M. Loghi, M. Poncino, and L. Benini. Cycle-accurate power analysis for multiprocessor systems-on-a-chip. In *Proc. of ACM Great Lakes symposium on VLSI*, pages 406–410, 2004.

[LSCS15] D. Liu, J. Spasic, G. Chen, and T. Stefanov. Energy-efficient mapping of real-time streaming applications on cluster heterogeneous mpsocs. In *ESTIMedia*, 2015.

[LSZ+14] D. Liu, J. Spasic, J. T. Zhai, T. Stefanov, and G. Chen. Resource optimization for csdf-modeled streaming applications

with latency constraints. In *Proceedings of the Conference on Design, Automation & Test in Europe*, DATE '14, pages 188:1–188:6, 3001 Leuven, Belgium, Belgium, 2014. European Design and Automation Association. URL: http://dl.acm.org/citation.cfm?id=2616606.2616837.

[LW82] J. Y.-T. Leung and J. Whitehead. On the complexity of fixed-priority scheduling of periodic, real-time tasks. *Performance Evaluation*, 2(4):237–250, 1982. doi:10.1016/0166-5316(82)90024-4.

[LW13] D. Li and J. Wu. Energy-aware scheduling for acyclic synchronous data flows on multiprocessors. *Journal of Interconnection Networks*, 14(4), 2013.

[Mar06] P. Marwedel. *Embedded System Design*. Springer-Verlag New York, Inc., Secaucus, NJ, USA, 2006.

[MB07] O. M. Moreira and M. J. G. Bekooij. Self-Timed Scheduling Analysis for Real-Time Applications. *EURASIP Journal on Advances in Signal Processing*, 2007(1), 2007. doi:10.1155/2007/83710.

[Mic] Xilinx Inc., MicroBlaze Soft Processor Core. http://www.xilinx.com.

[Mit15] T. Mitra. Heterogeneous multi-core architectures. *IPSJ Transactions on System LSI Design Methodology*, 8:51–62, 2015. doi:10.2197/ipsjtsldm.8.51.

[NMM+11] A. Nelson, O. Moreira, A. Molnos, S. Stuijk, B. T. Nguyen, and K. Goossens. Power minimisation for real-time dataflow applications. In *DSD*, 2011.

[NSD08] H. Nikolov, T. Stefanov, and E. Deprettere. Systematic and Automated Multiprocessor System Design, Programming, and Implementation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 27(3):542–555, 2008. doi:10.1109/TCAD.2007.911337.

[NVI15] NVIDIA. NVIDIA Tegra X1: NVIDIA'S New Mobile Superchip, 2015.

[ODR] ODROID. http://www.hardkernel.com.

[OH04] H. Oh and S. Ha. Fractional Rate Dataflow Model for Efficient Code Synthesis. *The Journal of VLSI Signal Processing*, 37:41–51, 2004. doi:10.1023/B:VLSI.0000017002.91721.0e.

[PDG06] J. Parkhurst, J. Darringer, and B. Grundmann. From single core to multi-core: Preparing for a new exponential. In *Proceedings of the 2006 IEEE/ACM International Conference on Computer-aided Design*, ICCAD '06, pages 67–72, New York, NY, USA, 2006. ACM. URL: http://doi.acm.org/10.1145/1233501.1233516, doi:10.1145/1233501.1233516.

[PMN+09] R. Pellizzoni, P. Meredith, M.-Y. Nam, M. Sun, M. Caccamo, and L. Sha. Handling mixed-criticality in SoC-based real-time embedded systems. In *Proceedings of the 7th ACM International Conference on Embedded Software*, EMSOFT '09, pages 235–244, New York, NY, USA, 2009. ACM. doi:10.1145/1629335.1629367.

[PP12] R. Piscitelli and A. D. Pimentel. A signature-based power model for mpsoc on fpga. *VLSI Design J.*, 2012(6), January 2012.

[PPKD10] S. Pasricha, Y.-H. Park, F. J. Kurdahi, and N. Dutt. Capps: A framework for power-performance tradeoffs in bus-matrix-based on-chip communication architecture synthesis. *IEEE Trans. on VLSI Systems*, 18:209–221, February 2010.

[PZMA04] O. U. Pereira Zapata and P. Mejía Alvarez. EDF and RM multiprocessor scheduling algorithms: Survey and performance evaluation. Technical Report CINVESTAV-CS-RTG-02, 2004.

[QKUP00] G. Qu, N. Kawabe, K. Usami, and M. Potkonjak. Function-level power estimation methodology for microprocessors. In *Proceedings of the 37th Annual Design Automation Conference*, DAC '00, pages 810–813, New York, NY, USA, 2000. ACM. URL: http://doi.acm.org/10.1145/337292.337786, doi:10.1145/337292.337786.

[RAN+11] S.K. Rethinagiri, R.B. Atitallah, S. Niar, E. Senn, and J.-L. Dekeyser. Hybrid system level power consumption estimation for fpga-based mpsoc. In *Proc. of IEEE ICCD*, pages 239–246, 2011.

[Sama] Samsung. Exynos 8 Octa (8890). URL: http://www.samsung.com/semiconductor/minisite/Exynos/w/solution/mod_ap/8890/ [cited June 8, 2016].

[Samb] Samsung. http://www.samsung.com.

[SC01] A. Sinha and A. P. Chandrakasan. Jouletrack - a web based tool for software energy profiling. In *Proc. of DAC*, pages 220–225, 2001.

[SDK13] A. K. Singh, A. Das, and A. Kumar. Energy optimization by exploiting execution slacks in streaming applications on multiprocessor systems. In *Proceedings of the 50th Annual Design Automation Conference*, DAC '13, pages 115:1–115:7, New York, NY, USA, 2013. ACM. URL: http://doi.acm.org/10.1145/2463209.2488875, doi:10.1145/2463209.2488875.

[SEL08] I. Shin, A Easwaran, and I. Lee. Hierarchical scheduling framework for virtual clustering of multiprocessors. In *Proceedings of 20th the Euromicro Conference on Real-Time Systems*, ECRTS '08, pages 181–190, 2008. doi:10.1109/ECRTS.2008.28.

[SGB06] S. Stuijk, M. Geilen, and T. Basten. SDF^3: SDF for free. In *Proc. of ACSD*, pages 276–278, 2006.

[SGB08] S. Stuijk, M. Geilen, and T. Basten. Throughput-buffering trade-off exploration for cyclo-static and synchronous dataflow graphs. *IEEE Trans. on Computers*, 57(10):1331–1345, 2008.

[SGTB11] S. Stuijk, M. Geilen, B. Theelen, and T. Basten. Scenario-aware dataflow: Modeling, analysis and implementation of dynamic applications. In *International Conference on Embedded Computer Systems (SAMOS), 2011*, pages 404–411, July 2011. doi:10.1109/SAMOS.2011.6045491.

[SJE11] M. Sackmann, D. Janssens, and P. Ebraert. A fast heuristic for scheduling parallel software with respect to energy and timing constraints. *2013 IEEE International Symposium on Parallel & Distributed Processing, Workshops and Phd Forum*, 00:1397–1406, 2011. doi:doi.ieeecomputersociety.org/10.1109/IPDPS.2011.284.

[SLA12] A. Stulova, R. Leupers, and G. Ascheid. Throughput driven transformations of synchronous data flows for mapping to heterogeneous MPSoCs. In *ICSAMOS*, pages 144–151. IEEE, 2012.

[SLCS15] J. Spasic, D. Liu, E. Cannella, and T. Stefanov. Improved hard real-time scheduling of csdf-modeled streaming applications. In *Proceedings of the 10th International Conference on Hardware/Software Codesign and System Synthesis*, CODES '15, pages 65–74, Piscataway, NJ, USA, 2015. IEEE Press. URL: `http://dl.acm.org/citation.cfm?id=2830840.2830848`.

[SLCS16] J. Spasic, D. Liu, E. Cannella, and T. Stefanov. On the improved hard real-time scheduling of cyclo-static dataflow. *ACM Transactions on Embedded Computing Systems*, 15(4):68:1–68:26, August 2016. URL: `http://doi.acm.org/10.1145/2932188`, `doi:10.1145/2932188`.

[SLS16a] J. Spasic, D. Liu, and T. Stefanov. Energy-efficient mapping of real-time applications on heterogeneous mpsocs using task replication. In *Proceedings of the 11th International Conference on Hardware/Software Codesign and System Synthesis*, CODES '16, pages 65–74, Piscataway, NJ, USA, 2016. IEEE Press. URL: `http://dl.acm.org/citation.cfm?id=2830840.2830848`.

[SLS16b] J. Spasic, D. Liu, and T. Stefanov. Exploiting resource-constrained parallelism in hard real-time streaming applications. In *2016 Design, Automation & Test in Europe Conference & Exhibition, DATE 2016, Dresden, Germany, March 14-18, 2016*, pages 954–959, 2016. URL: `http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=7459445`.

[SRH+11] M. Streubuhr, R. Rosales, R. Hasholzner, C. Haubelt, and J. Teich. Esl power and performance estimation for heterogeneous mpsocs using systemc. In *Proc. of the Forum on Specification, Verification and Design Languages*, pages 1–8, 2011.

[SS13] J. Spasic and T. Stefanov. An accurate energy model for streaming applications mapped on mpsoc platforms. In *2013 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, SAMOS 2013, Agios Konstantinos, Samos Island, Greece, July 15-18, 2013*, pages 205–212,

2013. URL: http://dx.doi.org/10.1109/SAMOS.2013.6621124, doi:10.1109/SAMOS.2013.6621124.

[TA10] W. Thies and S. Amarasinghe. An empirical characterization of stream programs and its implications for language and compiler design. In *Proceedings of the 19th International Conference on Parallel Architectures and Compilation Techniques*, PACT '10, pages 365–376, New York, NY, USA, 2010. ACM. doi:10.1145/1854273.1854319.

[TNS+07] M. Thompson, H. Nikolov, T. Stefanov, A. D. Pimentel, C. Erbas, S. Polstra, and E. F. Deprettere. A framework for rapid system-level exploration, synthesis, and programming of multimedia mp-socs. In *Proceedings of the 5th IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis*, CODES+ISSS '07, pages 9–14, New York, NY, USA, 2007. ACM. URL: http://doi.acm.org/10.1145/1289816.1289823, doi:10.1145/1289816.1289823.

[vHHK10] S. van Haastregt, E. Halm, and B. Kienhuis. Cost modeling and cycle-accurate co-simulation of heterogeneous multiprocessor systems. In *Proc.of DATE*, pages 1297–1300, 2010.

[VJD+07] A. Varma, B. Jacob, E. Debes, I. Kozintsev, and P. Klein. Accurate and fast system-level power modeling: An xscale-based case study. *ACM Trans. Embed. Comput. Syst.*, 6(4), September 2007. URL: http://doi.acm.org/10.1145/1274858.1274864, doi:10.1145/1274858.1274864.

[VNS07] S. Verdoolaege, H. Nikolov, and T. Stefanov. pn: a tool for improved derivation of process networks. *EURASIP Journal on Embedded Systems*, 2007(1):19–19, 2007. doi:10.1155/2007/75947.

[WBJS07] M. Wiggers, M. Bekooij, P. G. Jansen, and G. J. M. Smit. Efficient computation of buffer capacities for cyclo-static real-time systems with back-pressure. In *IEEE Real-Time and Embedded Technology and Applications Symposium*, pages 281–292. IEEE Computer Society, 2007.

[WYK+10] Y.-H. Wei, C.-Y. Yang, T.-W. Kuo, S.-H. Hung, and Y.-H. Chu. Energy-efficient real-time scheduling of multimedia tasks on

multi-core processors. In *Proceedings of the 2010 ACM Symposium on Applied Computing*, SAC '10, pages 258–262, New York, NY, USA, 2010. ACM. URL: http://doi.acm.org/10.1145/1774088.1774142, doi:10.1145/1774088.1774142.

[XKD12] H. Xu, F. Kong, and Q. Deng. Energy minimizing for parallel real-time tasks based on level-packing. In *Proceedings of the 2012 IEEE International Conference on Embedded and Real-Time Computing Systems and Applications*, RTCSA '12, pages 98–103, Washington, DC, USA, 2012. IEEE Computer Society. URL: http://dx.doi.org/10.1109/RTCSA.2012.10, doi:10.1109/RTCSA.2012.10.

[Yue91] M. Yue. A simple proof of the inequality FFD $(L) \leq 11/9$ OPT $(L) + 1, \forall L$ for the FFD bin-packing algorithm. *Acta Mathematicae Applicatae Sinica*, 7:321–331, 1991. doi:10.1007/BF02009683.

[YVKI00] W. Ye, N. Vijaykrishnan, M. Kandemir, and M. J. Irwin. The design and use of simplepower: A cycle-accurate energy estimation tool. In *Proceedings of the 37th Annual Design Automation Conference*, DAC '00, pages 340–345, New York, NY, USA, 2000. ACM. URL: http://doi.acm.org/10.1145/337292.337436, doi:10.1145/337292.337436.

[ZB09] F. Zhang and A. Burns. Schedulability Analysis for Real-Time Systems with EDF Scheduling. *IEEE Transactions on Computers*, 58(9):1250–1258, 2009. doi:10.1109/TC.2009.58.

[ZBS13] J. T. Zhai, M. A. Bamakhrama, and T. Stefanov. Exploiting just-enough parallelism when mapping streaming applications in hard real-time systems. In *Proceedings of the 50th Annual Design Automation Conference*, DAC '13, pages 170:1–170:8, New York, NY, USA, 2013. ACM. doi:10.1145/2463209.2488944.

[Zha15] J. T. Zhai. *Adaptive Streaming Applications: Analysis and Implementation Models*. PhD thesis, Leiden University, Netherlands, 2015.

[ZK00] C. L. Zitnick and T. Kanade. A cooperative algorithm for stereo matching and occlusion detection. *IEEE Trans. Pattern Anal. Mach. Intell.*, 22(7):675–684, July 2000. doi:10.1109/34.865184.

[ZSJ08] J. Zhu, I. Sander, and A. Jantsch. Energy efficient streaming applications with guaranteed throughput on mpsocs. In *Proceedings of the 8th ACM International Conference on Embedded Software*, EMSOFT '08, pages 119–128, New York, NY, USA, 2008. ACM. URL: http://doi.acm.org/10.1145/1450058.1450075, doi:10.1145/1450058.1450075.