Electrocatalysis at Single Nanoparticles

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Appendix A: Fabrication protocol

Chapters 3 and 4 discuss measurements performed on electrodes on microchips, that were specifically designed and fabricated for reproducible measurements of electrochemistry of nanoparticles. The fabrication process is described in detail and additionally design choices, as well as suggestions for future designs, are discussed.

The Fabrication of the on-chip nanoelectrodes was performed in the clean room at the Kavli Institute for Nanotechnology at Delft University of Technology. The process can be separated into two steps: (1) fabrication of Au conductive leads and (2) defining the area of Au nanoelectrodes by selectively etching away a passivation layer that prevents contact between the majority of the patterned Au area and the electrolyte.

Preparation of Au leads

Wafer cleaning

A 10 cm diameter silicon ((100); P-type, 10-30 Ω cm) wafer with a thermally grown oxide layer of 500 nm was purchased at the Van Leeuwenhoek Laboratory in Delft. Prior to processing, the wafer was first sonnicated in acetone for 30 seconds and then immersed in fuming HNO_3 for 5 minutes to oxidize any residual contamination on the wafer surface, and rinsed extensively with demineralized water (step 1 on the left-hand side of figure 1).

Application of electron-beam resist

Prior to applying the resist bi-layer for electron beam lithography (EBL) the wafer was baked on a hot plate for 5 minutes, to evaporate water from the wafer surface. After placing the wafer on the spin coater chuck, several milliliters of polymethylglutarimide (PMGI; 7% in cyclopentanone) were spread dropwise on its surface, using a microfiltered syringe, and it was spun to a thin layer at 2500 RPM and baked on a hot plate at 200℃ for 15 minutes. Immediately afterwards, a second layer of polymethylmethacrylate (PMMA; 950K, 2% in anisole) was spun at 6000 RPM and baked at 175℃ for 15 minutes (step 2).

e-beam exposure and pattern development

Patterns were defined into the resist bi-stack using a Vistec 5000+ electron beam pattern generator (EBPG), operating at 100kV. The pattern was developed in several steps. The PMMA layer was developed by immersing the wafer into a solution of

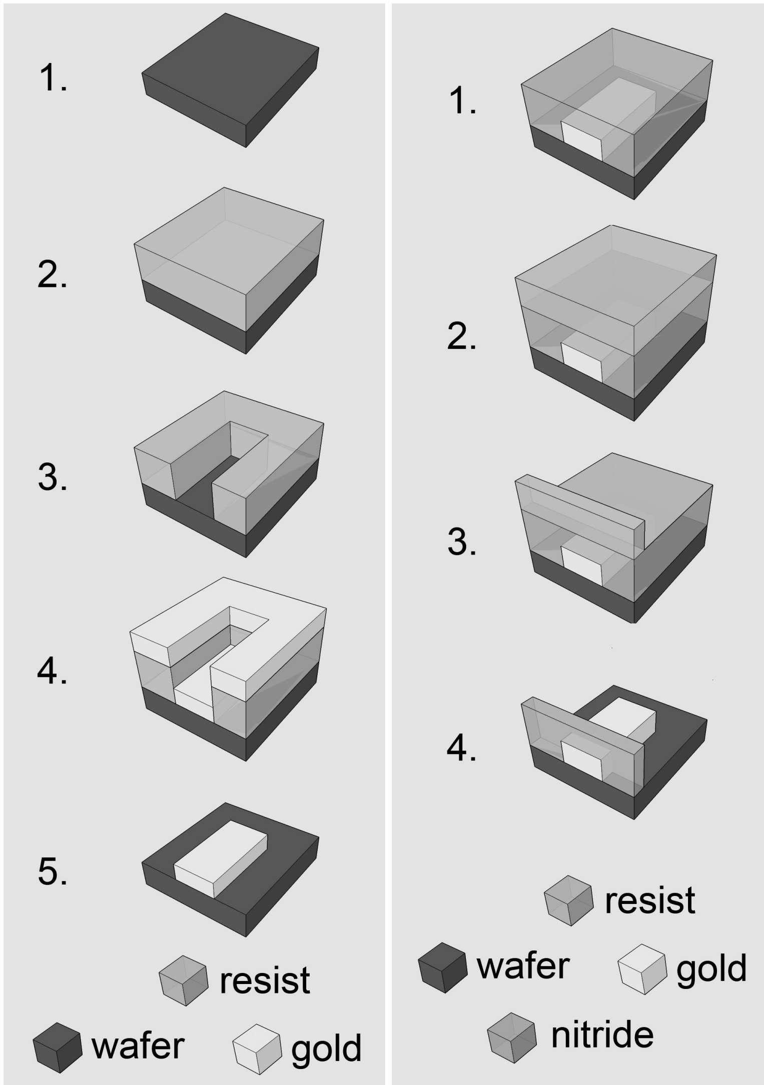

Figure 1: Stepwise formation of Au leads onto the Si wafer (left) and patterning the passivation layer to expose a part of the Au (right)

Methyl isobutyl ketone (MIBK) and isopropanol (IPA), mixed at a volume ratio of 1:3, for 60 seconds, followed by 30 seconds in an IPA bath to stop development. The PMGI layer was developed in Microposit MF-321 (based on Tetramethylammonium hydroxide) for 10 seconds followed by immersion in demineralized water for at least 15 seconds (step 3).

Metal evaporation and lift-off

After inspection of the pattern, the wafer was exposed to an oxygen plasma (50 cm^3min^{-1}; 100W) for 15 seconds, to remove any residual resist debris ('descumming'). Metal layers were then evaporated onto the wafer at a pressure of 5×10^{-7} mbar using a Temescal FC-2000 electron beam evaporation device. As an adhesion layer, 2 nm of Ti was evaporated at a rate of 1 $Ås^{-1}$, followed by 75 nm of Au at 1 $Ås^{-1}$(step 4). To lift off the resist-layer, the metallized wafer was immersed in a stirred bath of PRS-3000 (mainly 1-methyl-2-pyrrolidinone) at 85℃ for ~2 hours (step 5).

Passivation layer

Silicon nitride layer deposition and patterning

To passivate the Au leads, so that only a well-defined area of Au is in contact with the electrolyte, a layer of 400 nm of silicon nitride (Si_3N_4) was deposited using plasma-enhanced chemical vapor deposition (PECVD; Oxford Instruments Plasma Technology Plasmalab 80 Plus; step 1 in on the right-hand side of figure 1). Before a resist layer was spun onto the passivation layer, vinyl tape was applied to prevent resist from covering the macroscopic contact pads, to prevent either a lengthy electron beam patterning step or an additional photolithography step. Afterwards a thick layer of PMMA (950K, 7% in anisole) was spun at 1500 RPM and baked for 15 minutes at 175℃ (step 2). Windows were patterned in the resist using e-beam lithography, for which the location was defined using 20 $\times$ 20 μm^2 markers that were patterned along with the Au leads. The resist was developed in an MIBK and IPA bath (1:3) for 100 seconds, during which ultrasound agitation was applied for 20 seconds, followed by immersion in IPA for at least 30 seconds (step 3).

Dry etching and wafer dicing

The window patterned in the resist layer was transferred into the Si_3N_4 passivation layer by resistive ion etching (RIE; dry etching). Dry etching occurred in a plasma of CHF_3 (50 cm^3min^{-1}) and O_2 (2.5 cm^3min^{-1}) at a chamber pressure of 9 µbar and

50W power (step 4). To follow the etching process, the wafer was examined using a Woollam spectroscopic ellipsometer (J.A. Woollam co. inc., M2000XI), at different time intervals, which revealed an etch rate of approximately 40 nm min^{-1}. Before the wafer was diced into 25 microchips, it was cleaned by immersion in fuming HNO_3 and covered with a layer of Shipley S1813 resist (5000 RPM; 15 minutes at 120 ℃) to prevent excessive Si dust spreading during sawing. After dicing the chip was transferred for measurement to Leiden University.

Discussion

The optimization of lithographically produced devices is a lengthy cycle of prototype preparation, testing and improvement. While the present state of the design is well suited for electrochemical measurements, for lack of time some improvements were not made during the course of the research described in this thesis. Some suggestions are listed here, as well as justifications for several of the fabrication steps from the above.

For the lift-off step, a bi-stack of electron beam resists was applied. Two different resists were used, that both have separate development processes. The bottom, PMGI layer is developed to have a slightly wider pattern than the PMMA on top and is also thicker than the PMMA film. This arrangement prevents the adhesion of metal deposits to the side-walls of the pattern and allows for enhanced solvent access during lift-off. The recipe and the resist stack chosen was the standard protocol provided for lift-off processes by the VLL clean room staff.

The electrodes were patterned in Au because this is the most inert metal that can be conveniently processed in the clean room. Au electrodes are very resistant to chemical cleaning methods, such as immersion in highly oxidative “piranha” mixtures, and can be routinely characterized electrochemically to verify both the cleanliness of the surface and the electrochemically active surface area, as described in chapter 3. The latter is a good verification of a successful fabrication. Au films do not adhere well to the silicon oxide layer on which they are patterned. Typically, an intermediate layer of Cr or Ti is deposited on the SiO_x first, since these metals form strong, chemical bonds with the oxide layer and a metallic interaction with the Au film deposited on top. During measurements of Au nanoelectrodes with Cr as an intermediate layer, parasitic electronic signals were measured that were tentatively attributed to Cr redox chemistry. Upon changing the intermediate layer to Ti, these parasitic signals were lost.

Au electrodes are quite inert, but carbon substrates are known to show even fewer background signals. Particularly for catalytic reactions such as the oxygen reduction

reaction, or the oxidation of hydrazine, carbon electrodes will participate less than Au electrodes. Very interesting measurements using single carbon nanotubes have been demonstrated, although this adds significant additional complexity to fabrication.[1] An alternative, patternable, carbon substrate can be made by pyrolizing a patterned resist layer after development. This has been demonstrated to reproducibly yield carbon microband electrodes.[2]

The passivation layer is made out of silicon nitride. Initially, vapour deposited silicon oxide films were attempted, but these showed signs of electrolyte leakage to the Au leads. While no further investigation was performed, it was assumed that such SiO_x films are mesoscopically porous and therefore transparent to aqueous solutions.

As described in chapter 3, significant efforts were undertaken to suppress parasitic capacitance from the silicon underneath the SiO_x layer. This capacitance could be prevented by patterning the Au leads on an insulator, for instance by using a glass wafer, as was demonstrated by Ferrari et al..[3] It should be noted that glass wafers charge up during electron beam patterning, significantly reducing the resolution of the process.

The flow cell environment used in the measurements described in chapters 3 and 4 has poor atmospheric control. Therefore, the electrochemical measurements are hindered by the presence of oxygen gas. Significant improvements of atmospheric control have been shown through the construction of specialized measurements cells,[4] and similar setups will be beneficial for future measurements on the microchips described in this thesis.

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