Adaptive streaming applications : analysis and implementation models

Zhai, J.T.

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Jiali Teddy Zhai
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Leiden, The Netherlands

Curriculum Vitae

Jiali Teddy Zhai was born on 16^{th} of October, 1982. In September 2009, he received Diplom Informatik (Master Degree in Computer Science) from Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany. During his study, Teddy worked at Institute for Hardware-Software-Co-Design headed by Prof. Jürgen Teich with the focus on designing high-level synthesis tools targeting high-performance computing systems based on FPGA platforms. In October 2009, Teddy joined the Leiden Embedded Research Center (LERC) which is part of the Leiden Institute of Advanced Computer Science (LIACS) at Leiden University. He was appointed as a research and teaching assistant (Ph.D. student). He was involved in the NEtherlands STreaming (NEST) project in collaboration with NXP semiconductor, Philips Healthcare, etc. The research work culminated in the writing of this Ph.D. dissertation in 2013.

List of Publications

Journal Article

- **Jiali Teddy Zhai**, Hristo Nikolov, and Todor Stefanov, "Mapping of Streaming Applications considering Alternative Application Specifications", in ACM Transactions on Embedded Computing Systems (TECS), vol. 12, Issue 1s, Article 34, March 2013.

Peer-Reviewed Conference Proceedings

- **Jiali Teddy Zhai**, Mohamed A. Bamakhrama, Todor Stefanov, "Exploiting Just-enough Parallelism when Mapping Streaming Applications in Hard Real-time Systems", *In the Proceedings of the 50th IEEE/ACM Design Automation Conference (DAC'13)*, pp. 170:1–170:8, Austin, TX, USA, June 2 - 6, 2013. **WINNER of the 2013 HiPEAC Paper Award!**
- **Jiali Teddy Zhai**, Hristo Nikolov, Todor Stefanov, "Mapping Streaming Applications considering Alternative Application Specifications (Extended Abstract)", *In Proceedings of the 10th IEEE Symposium on Embedded System for Real-Time Multimedia (ESTIMedia'12)*, Tampere, Finland, October 11-12, 2012.
- Mohamed A. Bamakhrama, **Jiali Teddy Zhai**, Hristo Nikolov, Todor Stefanov, "A Methodology for Automated Design of Hard-Real-Time Embedded Streaming Systems", *In Proceedings of the Conference on Design, Automation and Test in Europe (DATE'12)*, pp. 941–946, Dresden, Germany, March 12-16, 2012.
- **Jiali Teddy Zhai**, Hristo Nikolov, Todor Stefanov, "Modeling Adaptive Streaming Applications with Parameterized Polyhedral Process Networks", *In the Proceedings of the 48th IEEE/ACM Design Automation Conference (DAC'11)*, pp. 116–121, San Diego, CA, USA, June 5-9, 2011. **WINNER of the 2011 HiPEAC Paper Award!**

Peer-Reviewed Workshop Proceeding

- Mohamed A. Bamakhrama, **Jiali Teddy Zhai**, Todor Stefanov, "An Optimal Design Flow for Hard Real-Time Streaming Systems", *In the Proceedings of the 7th Junior Researcher Workshop on Real-Time Computing (JRWRTC'2013)*, in conjunction with the 21st International Conference on Real-Time and Network Systems (RTNS 2013), Sophia Antipolis, France, October 16-18, 2013.

Publications not Covered in this Thesis

- Di Liu, Jelena Spasic, **Jiali Teddy Zhai**, Gang Chen, and Todor Stefanov, "Resource Optimization for CSDF-modeled Streaming Applications with Latency Constraints", *In Proceedings of the Conference on Design, Automation and Test in Europe (DATE'14)*, Dresden, Germany, March 24-28, 2014.
- Mohamed A. Bamakhrama, **Jiali Teddy Zhai**, "Daedalus/Daedalus^{RT} User Manual", September 2012, the manual can be downloaded from `http://daedalus.liacs.nl/manual.pdf`
- Hritam Dutta, **Jiali Teddy Zhai**, Frank Hannig, Jürgen Teich, "Impact of Loop Tiling on the Controller Logic of Acceleration Engines", *In Proceedings of 20th IEEE International Conference on Application-specific Systems, Architectures, and Processors (ASAP)*, Boston, MA, USA, July 7-9, 2009.

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List of Abbreviations

CPU	Central Processing Unit
CSDF	Cyclo-Static Data Flow
DLP	Data-Level Parallelism
DSP	Digital Signal Processing
EDF	Earliest Deadline First
ESL	Electronic System Level
FFD	First-Fit Decreasing
Gbps	Giga-bit per second
GPU	Graphic Processing Unit
HRT	Hard Real Time
Kbps	Kilo-bit per second
MADF	Mode-Aware Data Flow
Mbps	Mega-bit per second
MoC	Models of Computation
MPSoC	Multi-Processor System-on-Chip
NoC	Network-on-Chip
PE	Processing Element
PLP	Pipeline-Level Parallelism

RM	Rate Monotonic
SDR	Software-Defined Radio
SIMD	Single Instruction Multiple Data
TLP	Task-Level Parallelism
WCDMA	Wideband Code Division Multiple Access
WCET	Worst Case Execution Time